

VER : 1A  
PWA:  
PWB:

**FAN & THERMAL**  
EMC2112 PG 37

REGULATOR	
+1.5V_SUS/+0.75V_DDR_VTT	PG 46
+1.05V_VTT	PG 47

<b>CPU VR</b>	PG 43
<b>DC/DC</b> +3.3V_ALW/+5V_ALW/ +15V_ALW	PG 44
<b>VGA Core</b>	PG 49





 <b>Quanta Computer Inc.</b> <b>PROJECT : GM6C MLK DIS</b>		
Size	Document Number	Rev
	<b>Block Diagram</b>	1A
Date:	Friday, January 07, 2011	Sheet 1 of 59

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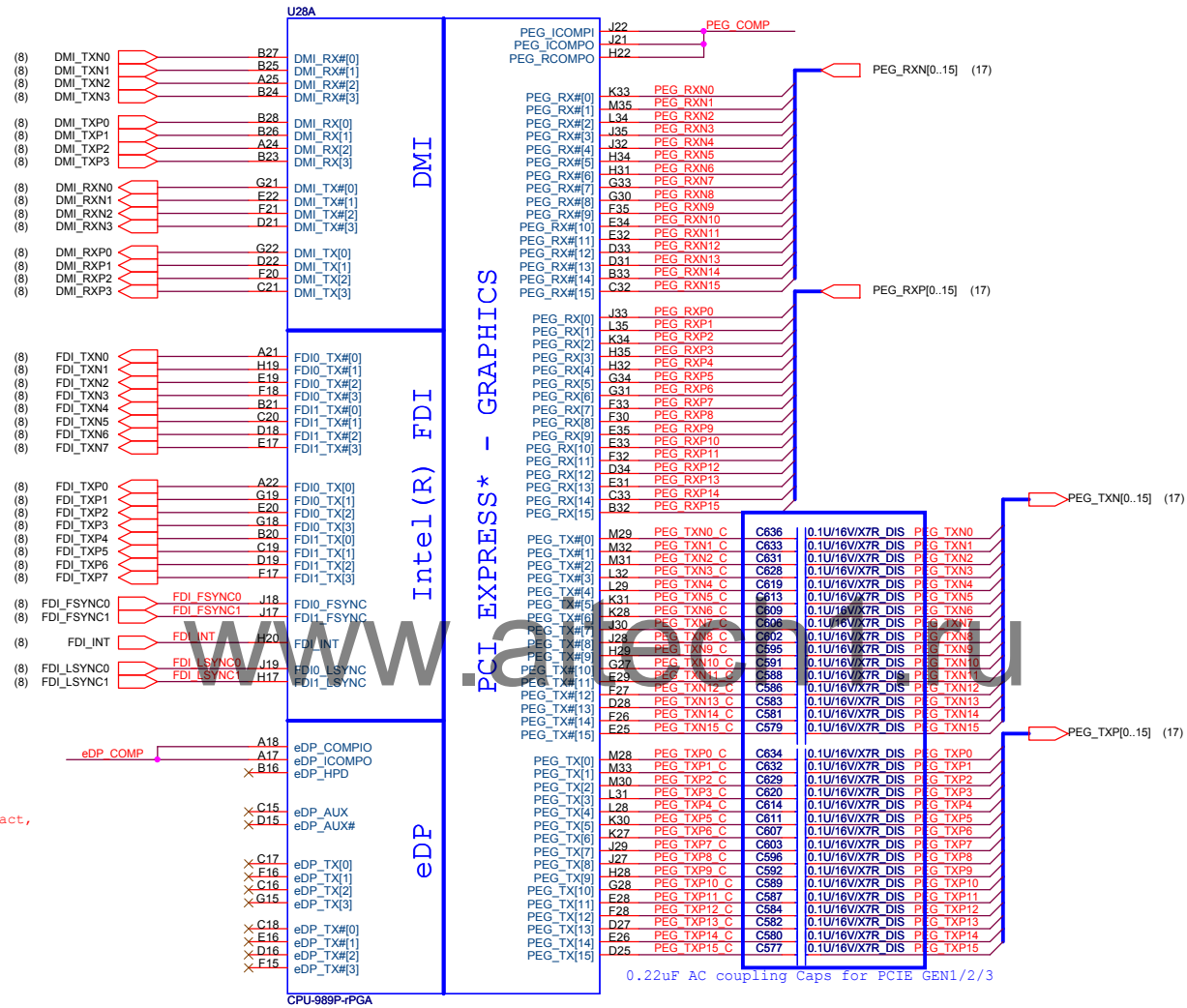
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-7	Sandy Bridge
8-14	PCH
15-16	DDRIII SO-DIMM(204P)
17-21	N12P-GE/N12P-GT
22-23	VRAM
24	LCD CONN
25	HDMI CONN
26	MINI DP CONN
27	Card Reader (JMB389)
28	SIO (ITE8502)
29	MINI-Card (WLAN/WPAN)
30	MINI-Card (WWAN)
31	LAN(RTL8111EL/RJ-45)
32	Right USB/ESATA
33	SATA (HDD & ODD)
34	TP / KEYBOARD
35	SWITCH / LED / T-Screen
36	FLASH / RTC/ RESET CIRCUIT
37	FAN / THERMAL
38	AUDIO CODEC
39	AUDIO AMP
40	Left USB/MMB CONN
41	BLANK
42	Charger (ISL8731)
43	CPU CORE(NCP6131S)
44	3V/5V (TPS51427A)
45	1.8V_RUN(RT8015DGQW)
46	1.5_DDR/0.75(RT8207A)
47	1.05V_VTT(VT358)
48	VCCSA(TPS51461)
49	VGA_N12x-dGFX(NCP3218MNR)
50	Run Power Switch
51	DCin & Batt
52	PAD & SCREW
53	SMBUS BLOCK
54	THERMAL MAP
55	Power Block Diagram
56	Power sequence Block
57	power sequence(DIS)
58	power sequence(UMA)
59	power sequence(OPTIMUS)

Power States

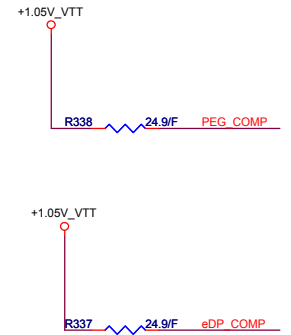
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

# Sandy Bridge Processor (DMI, PEG, FDI)

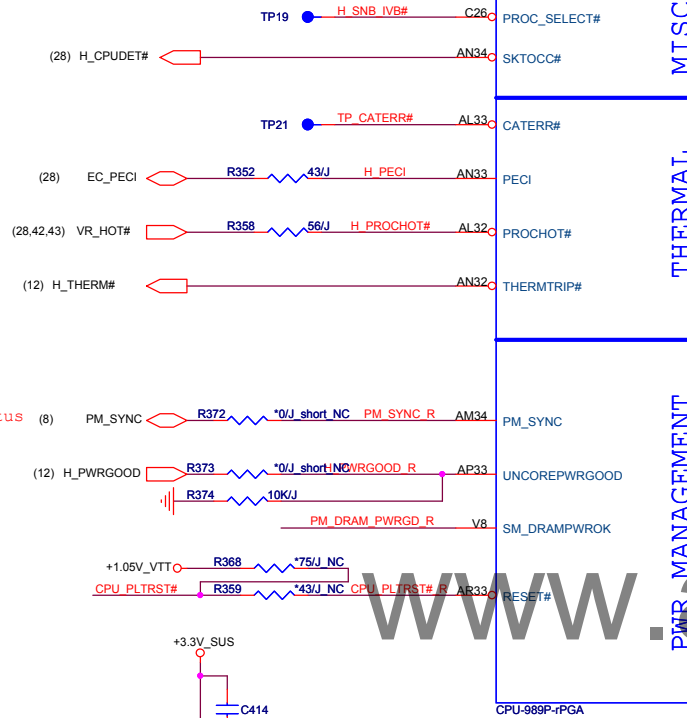


## DP & PEG Compensation



# Sandy Bridge Processor (CLK,MISC,JTAG)

WW31.MOW Page 5 (SNB\_IVB# N.A at SNB EDS #27637 0.7v1)



shut down when asserted  
Over 130 degree C will  
drive low

	DIS	SW
Ra	NA	0 ohm
Rb	1K ohm	NA
Rc	1K ohm	NA

26.1 change to 25 ohm

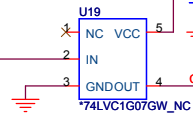


Option for Prochot# function  
68 ohm for unused, 62 ohm for used



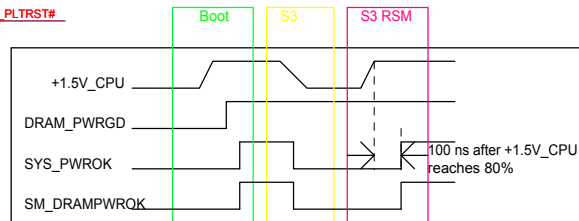
IN	OUT
L	L
H	High-Z

(11,17,27,28,29,30,31,40) PLTRST#



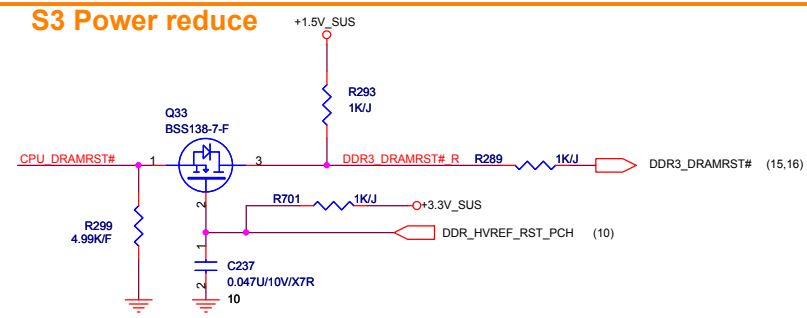
level shift for reset pin(07/12)

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	High-Z

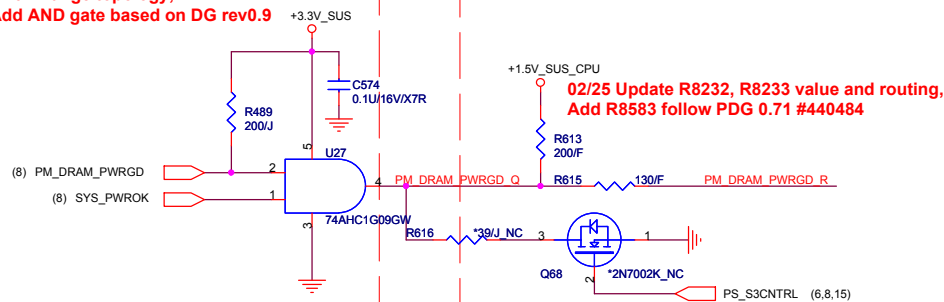


+1.5V\_SUS keep DDR3\_DRAMRST# high to avoid CPU\_DRAMRST# low when into S3  
(Because can't reset DRAM when into S3)

## S3 Power reduce



3/16 Change topology;  
Add AND gate based on DG rev0.9



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PROJECT : GM6C MLK DIS

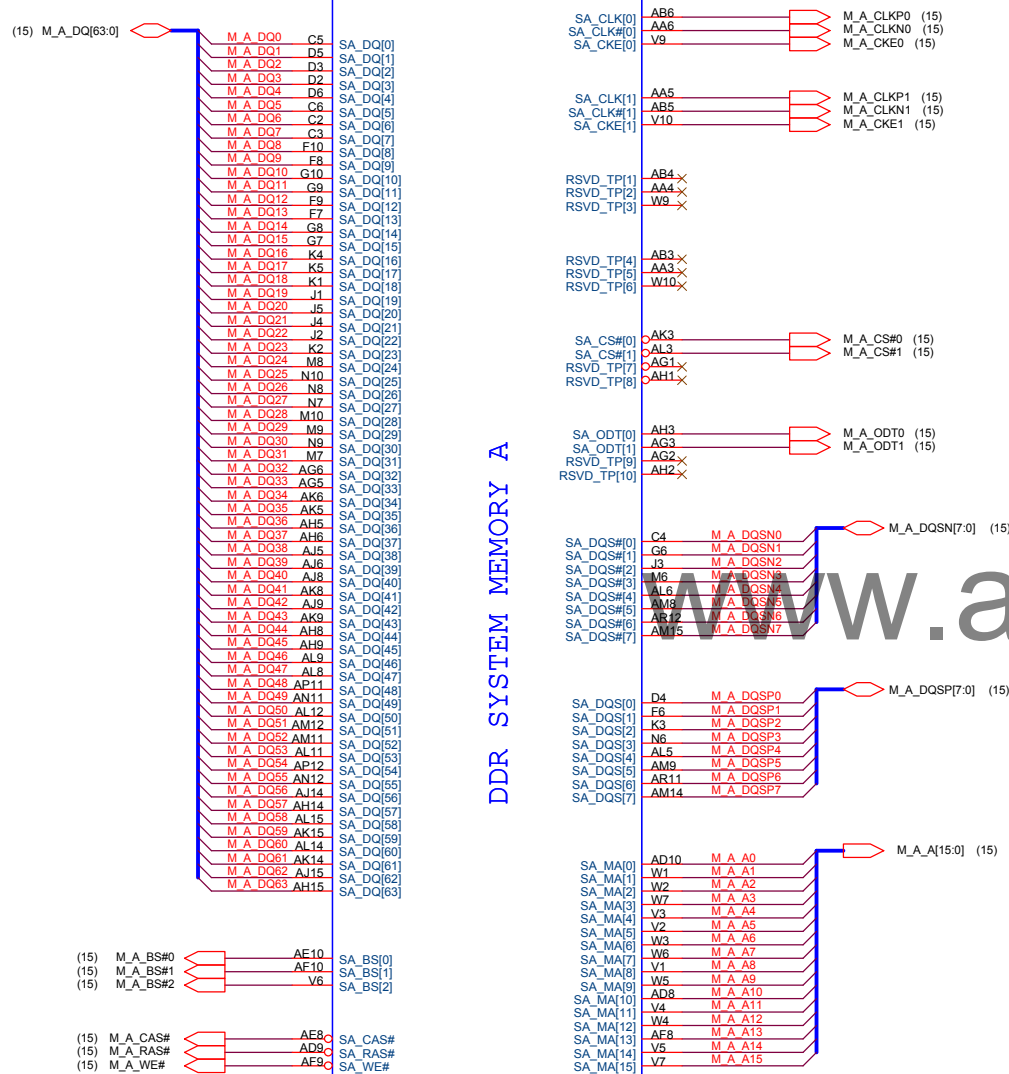
Size	Document Number	Rev
	Sandy Bridge 2/5	1A
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# Sandy Bridge Processor (DDR3)

U28C

CPU-989P-IPGA

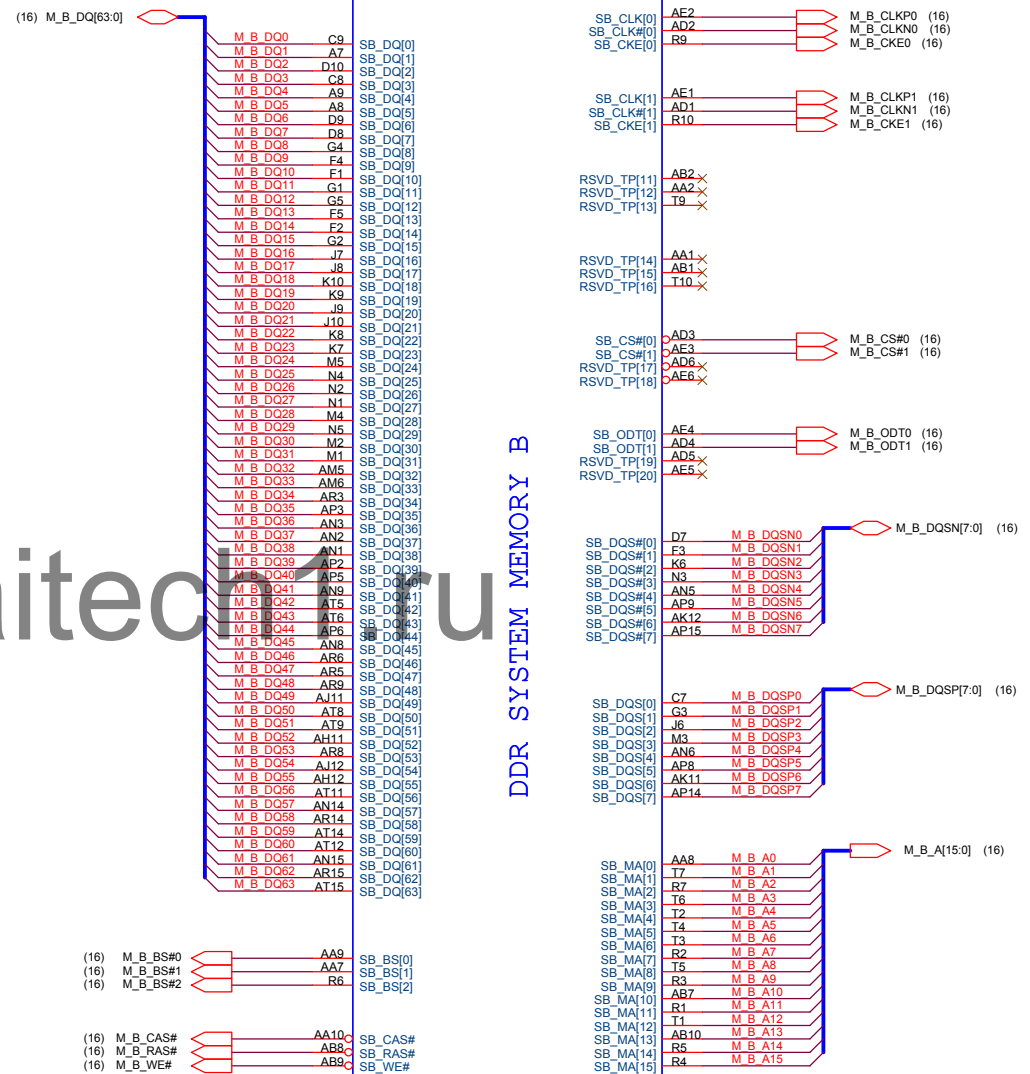
DDR SYSTEM MEMORY A



U28D

CPU-989P-IPGA

DDR SYSTEM MEMORY B

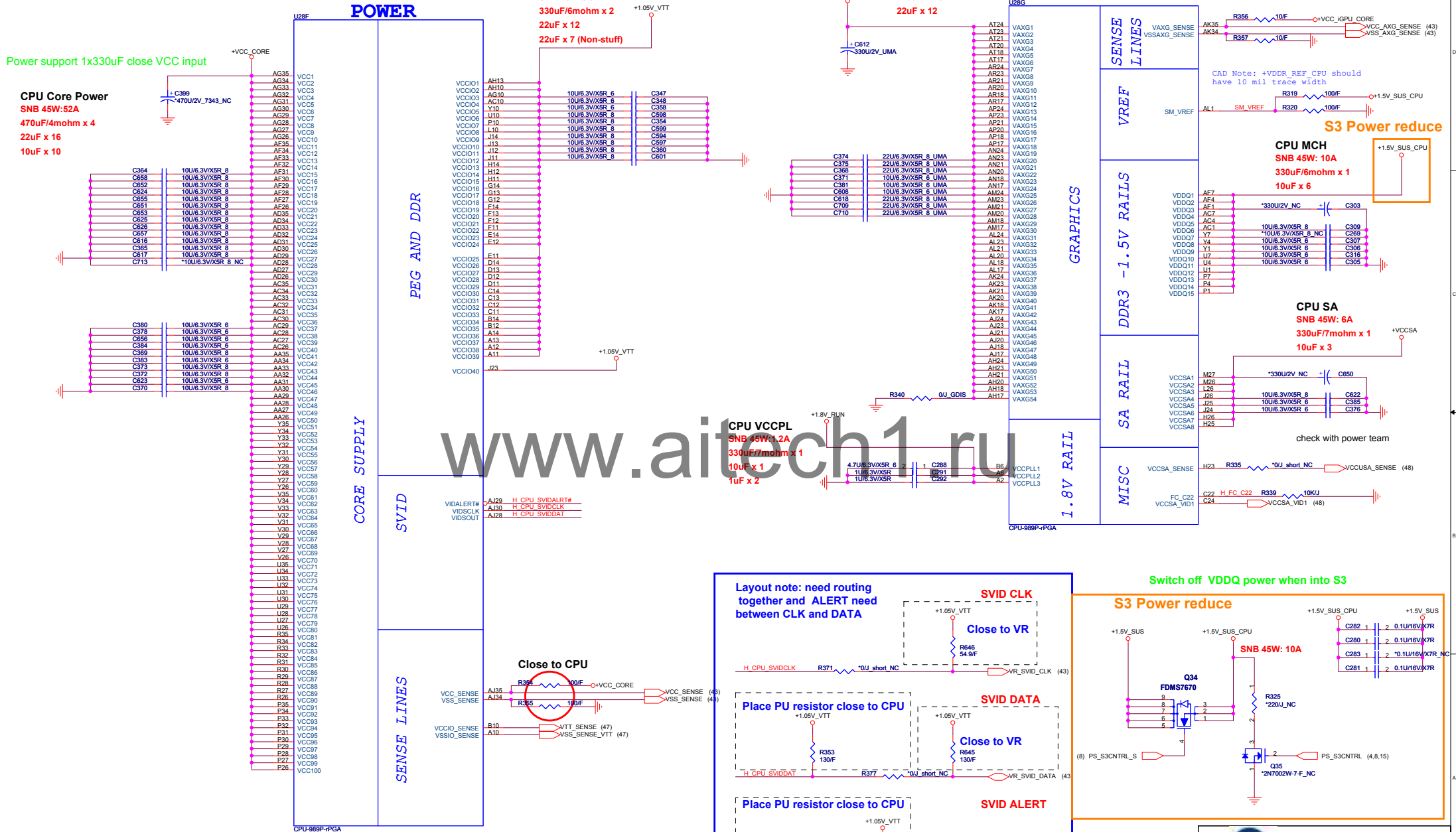


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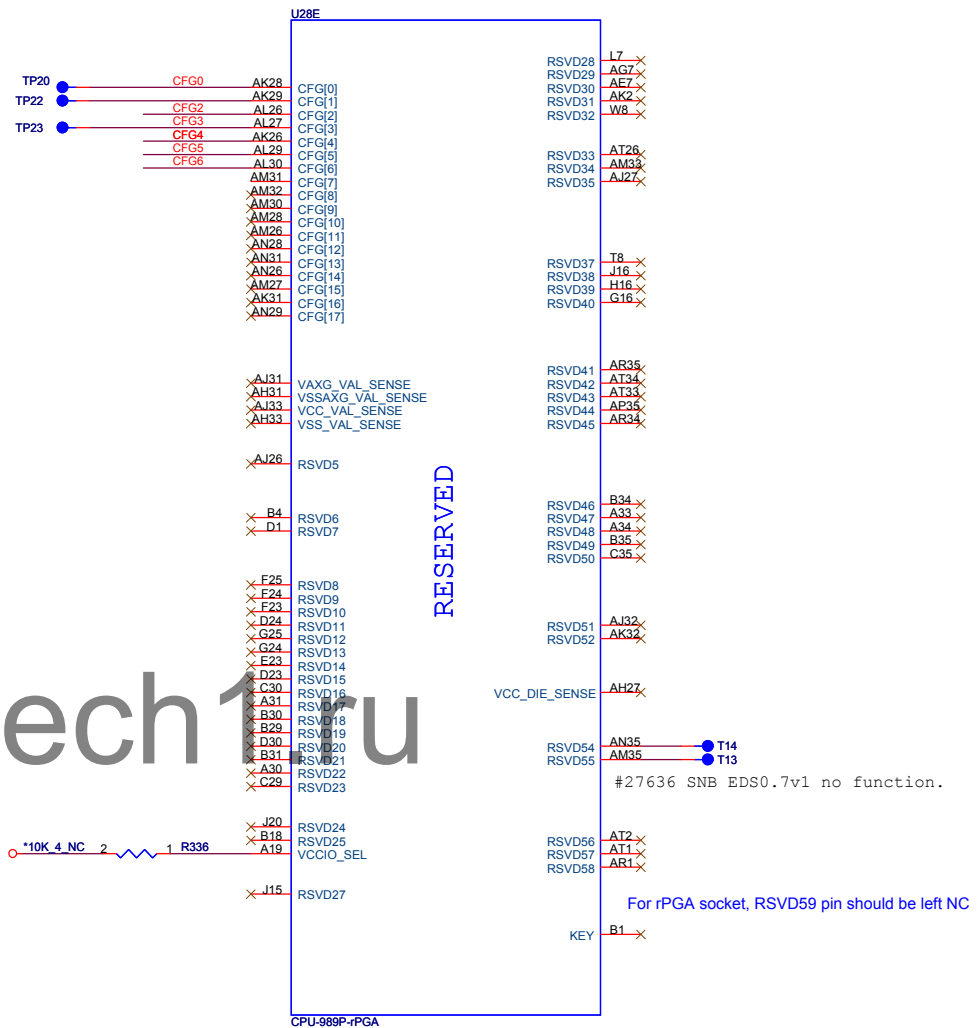
PROJECT : GM6C MLK DIS

## Sandy Bridge Processor (POWER)

## Sandy Bridge Processor (GRAPHIC POWER)



**Sandy Bridge Processor (RESERVED, CFG)**



The CFG signals have a default value of '1' if not terminated on the board.

CFG2 R342 1K/F

CFG3 R370 \*1K/F\_NC

CFG4 R361 \*1K/F\_NC

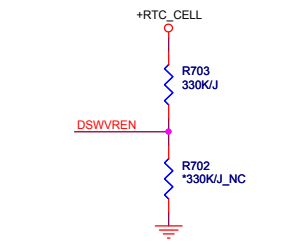
CFG[6:5] (PCIe Port Bifurcation Straps)

```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```



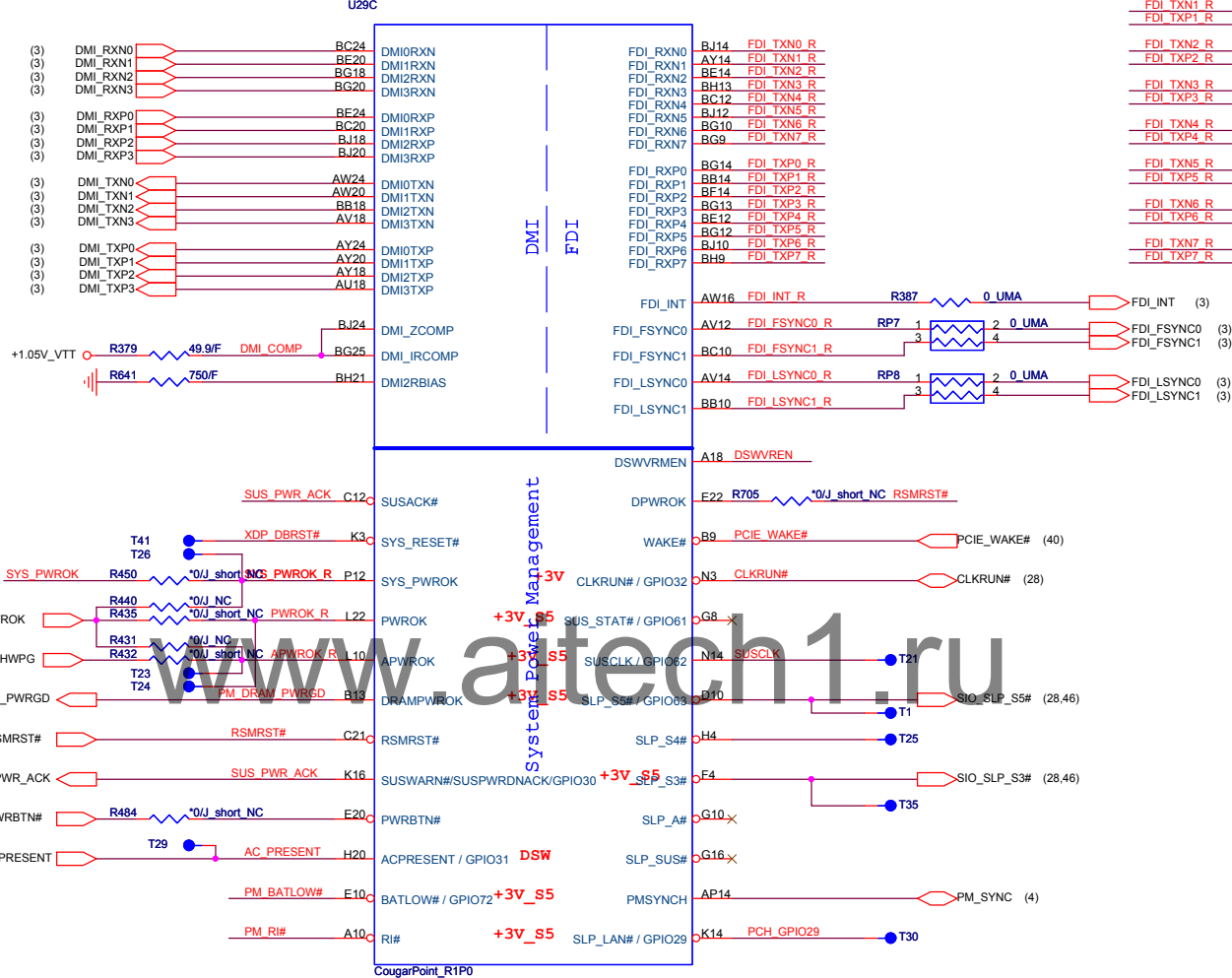
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	<b>Sandy Bridge 5/5</b>	1A
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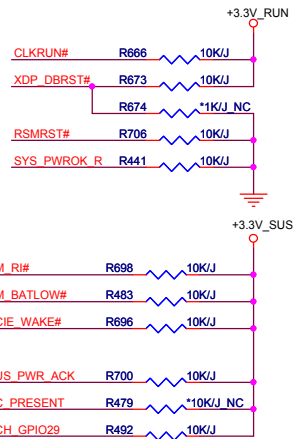


On Die DSW VR Enable  
 High = Enable (Default)  
 Low = Disable

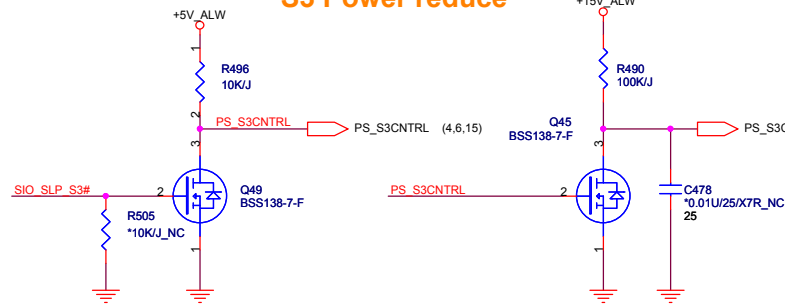
## Cougar Point (DMI, FDI, PM)



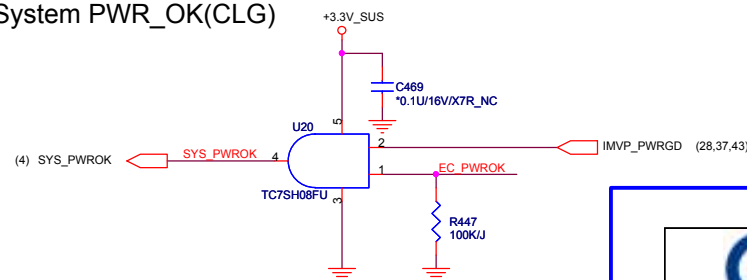
## PCH Pull-high/low(CLG)



## S3 Power reduce



## System PWR\_OK(CLG)



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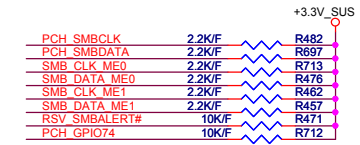
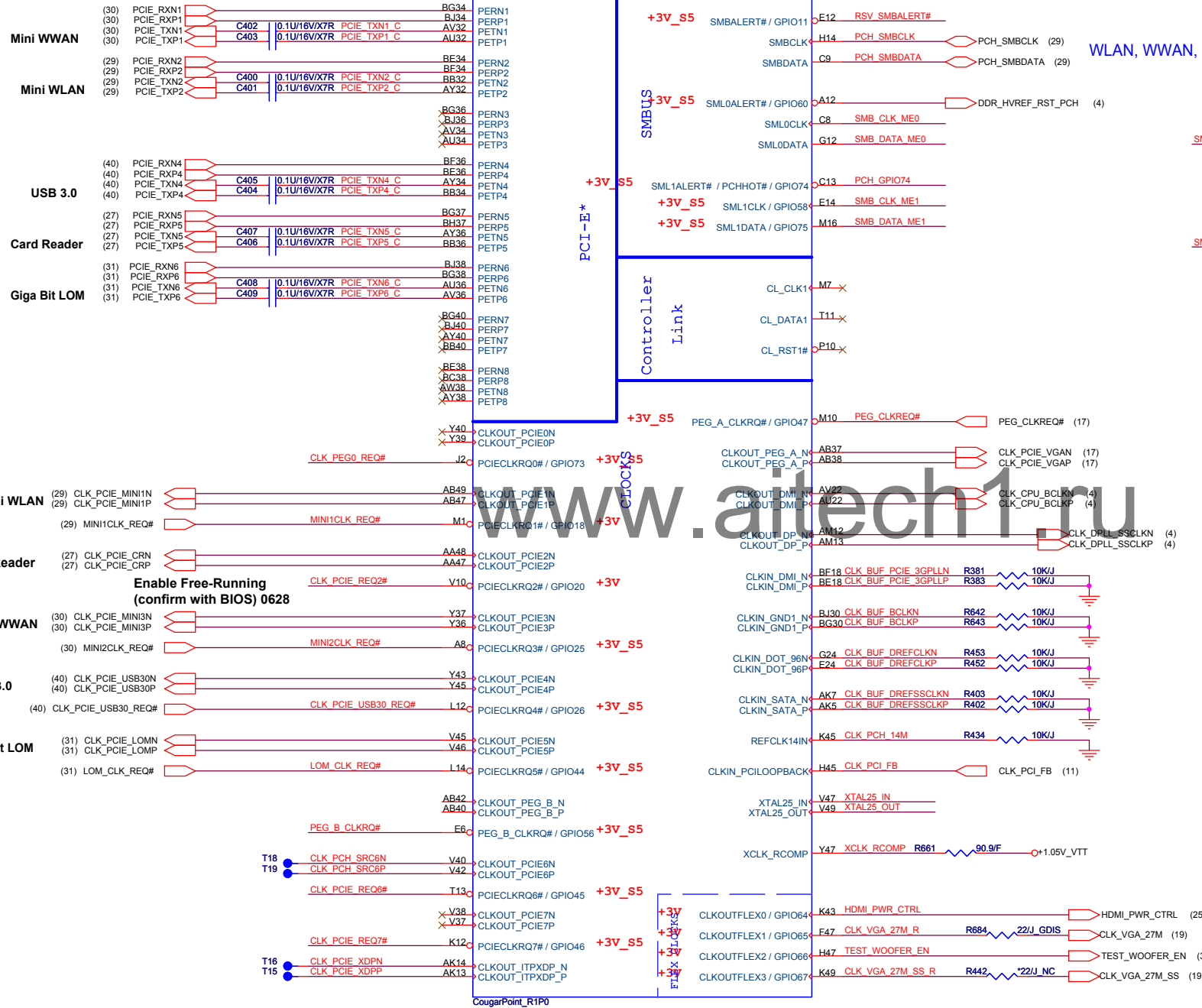
**PROJECT : GM6C MLK DIS**



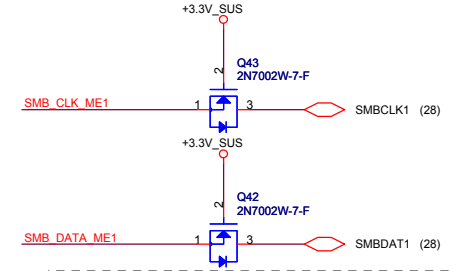
# Cougar Point-M (PCI-E, SMBUS, CLK)

Note: Place TX DC blocking caps close to PCH.

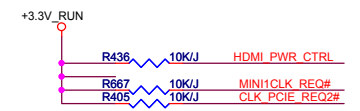
U298



WLAN, WWAN, DIMM0, DIMM1, 3-axis fall sensor



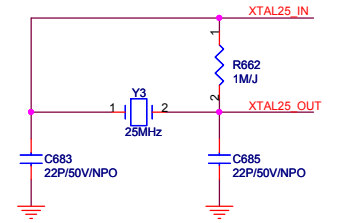
## PCIe Clock Request



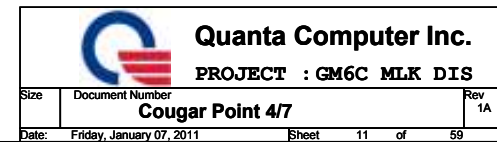
PCIECLKRQ[0,3,4,5,6,7]# should have a 10K pull-up to +V3.3A. PCIECLKRQ[1,2] should have a 10K pull-up to +3.3S

## Change as big package (UM9)

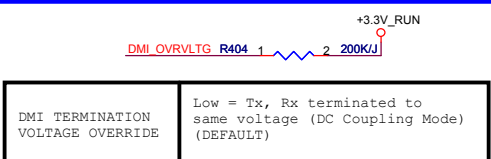
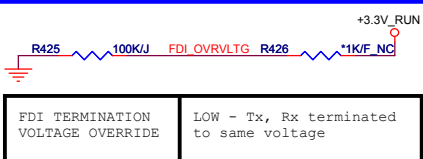
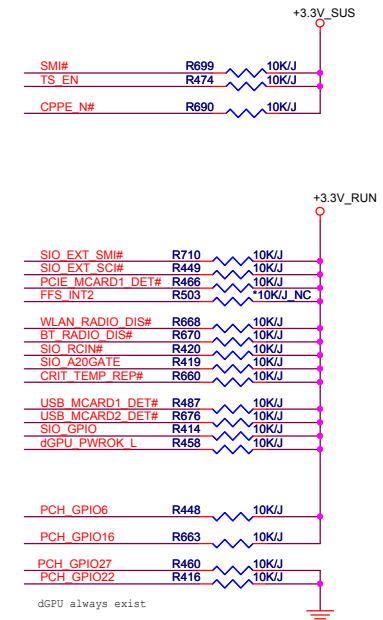
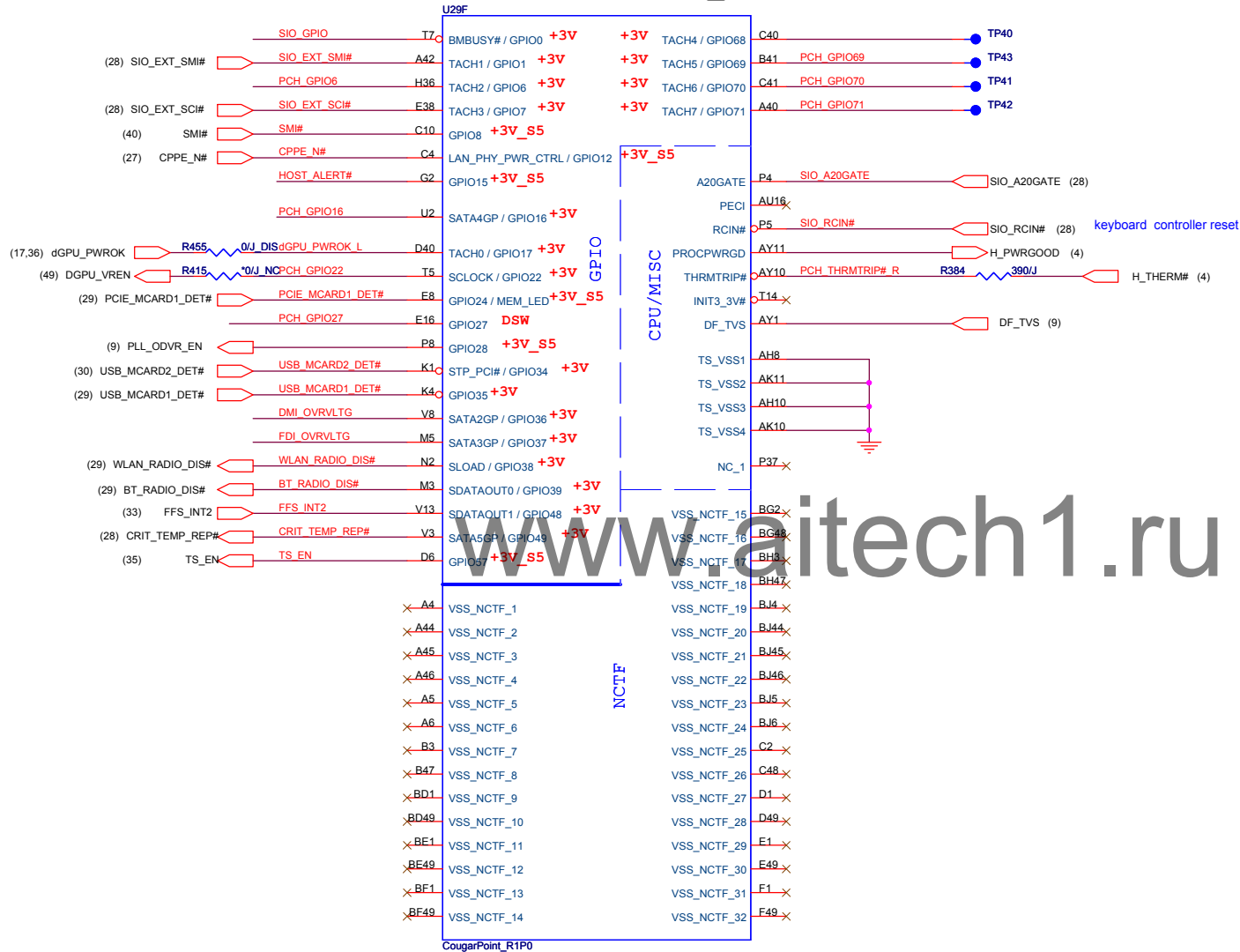
### 25MHz Clock for DCI Function



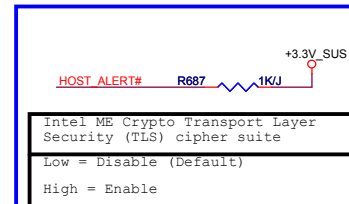
Cougar Point-M (PCI,USB,NVRAM)



# Cougar Point (GPIO,VSS\_NCTF,RSVD)

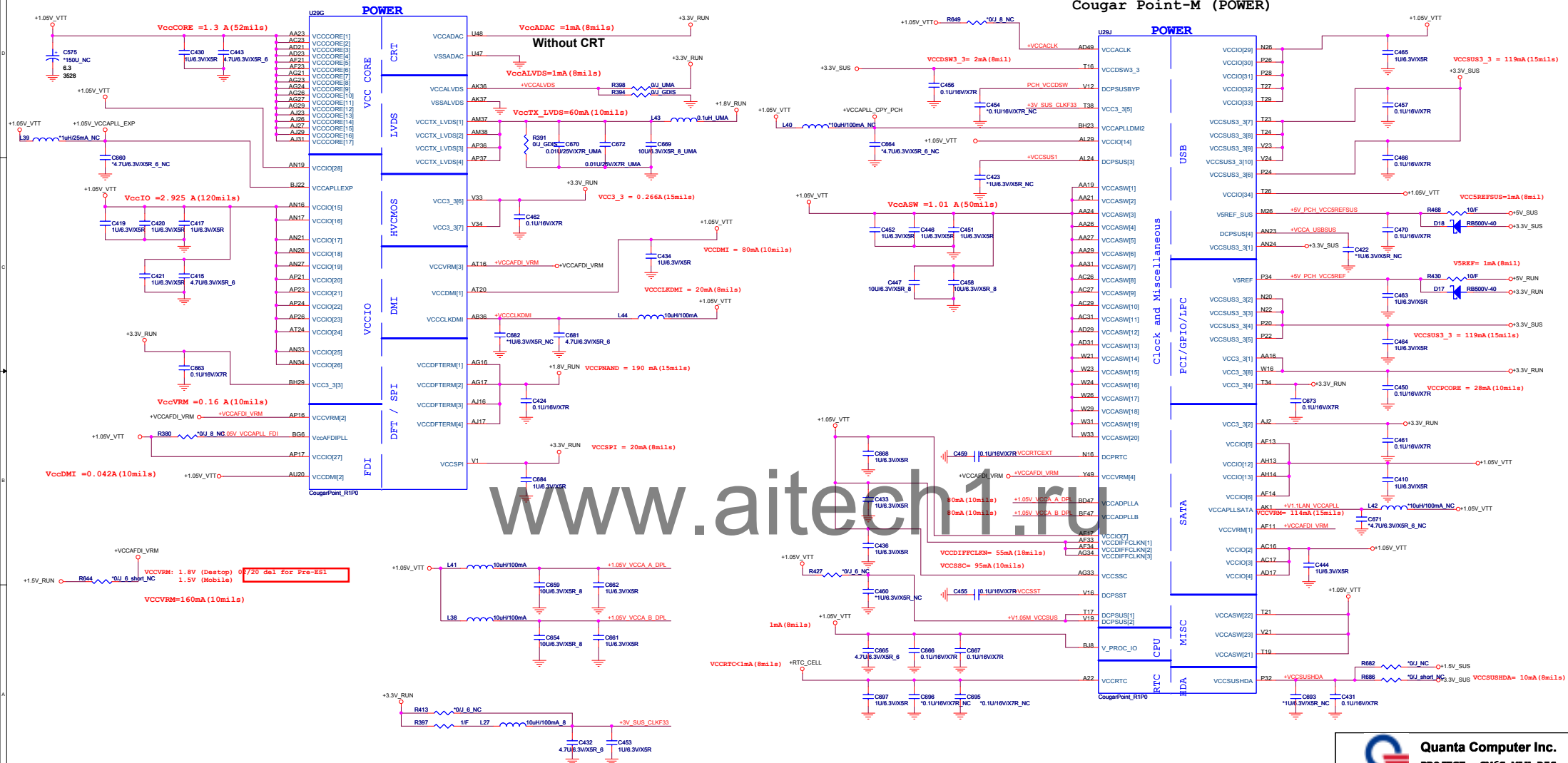


internal PD resistor 20K-ohm  
To avoid voltage be divided,  
please change GPIO36 PU resistor from  
10K-ohm to 200K-ohm. (07/12)

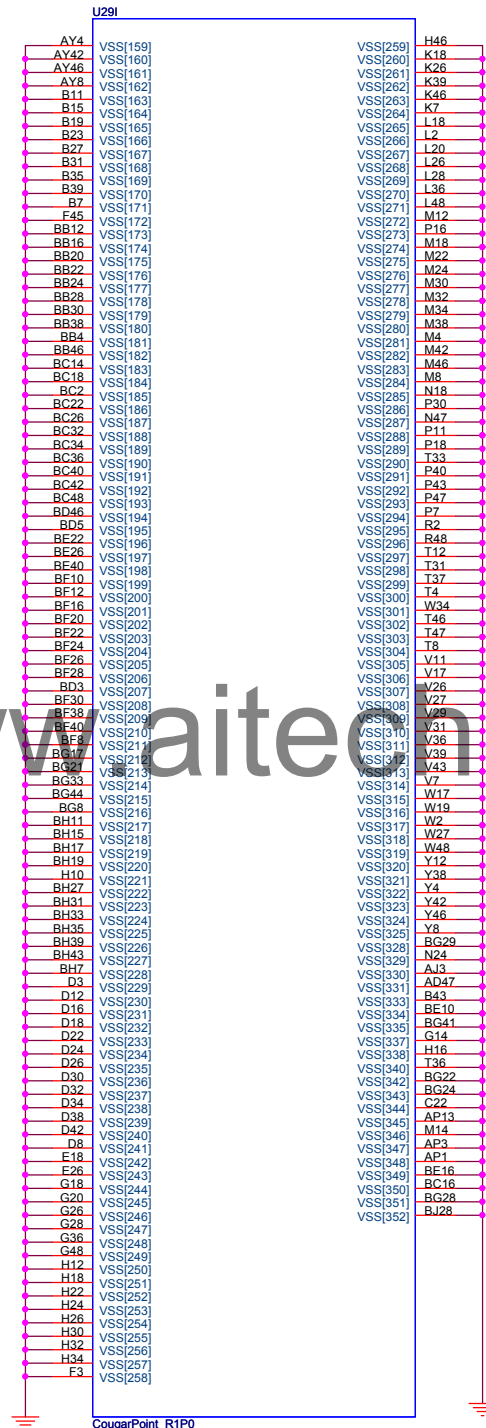
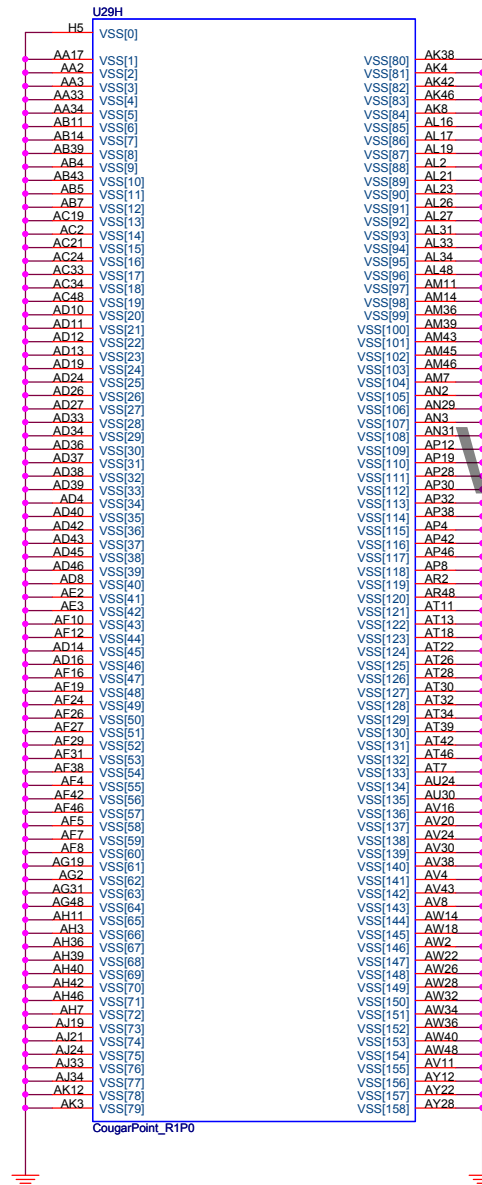


**Quanta Computer Inc.**  
**PROJECT : GM6C MLK DIS**

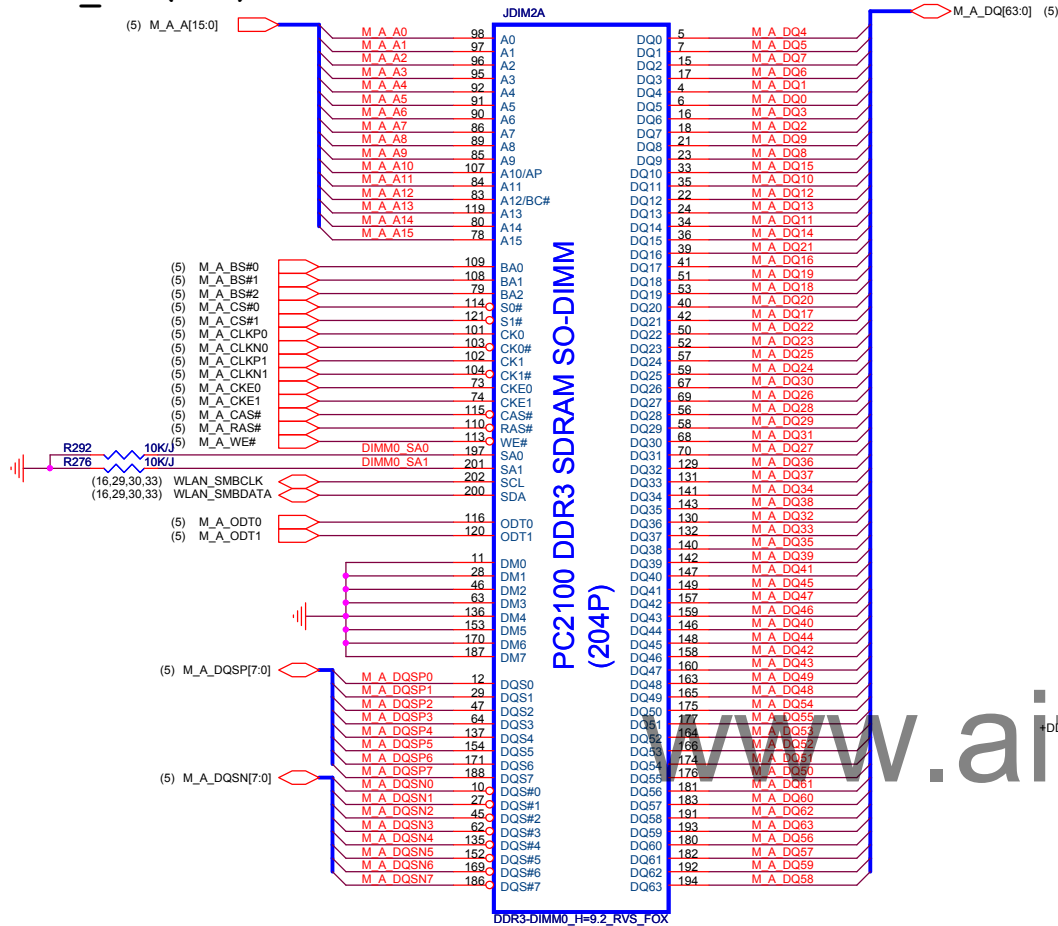
Cougar Point-M (POWER)



## IBEX PEAK-M (GND)

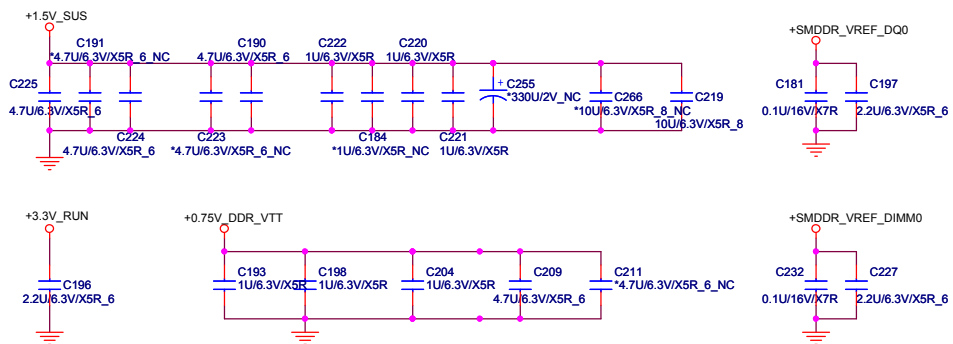


# DDR STD (DDR)

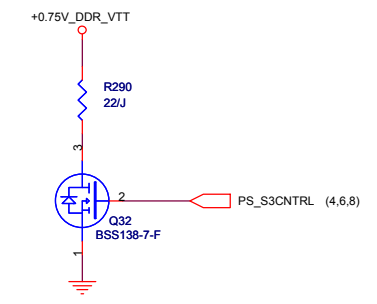


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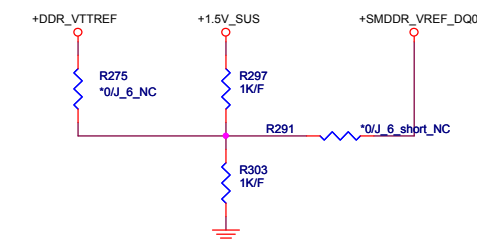
## Place these Caps near So-Dimm0.



## S3 Power reduce



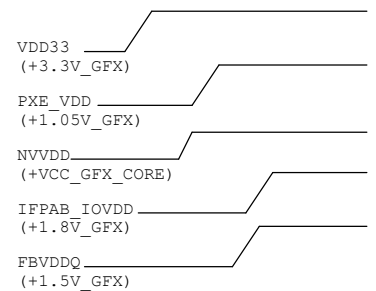
## M1 VREF Solution



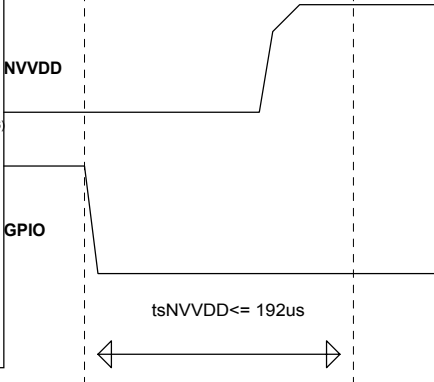
**Quanta Computer Inc.**  
PROJECT : GM6C MLK DIS



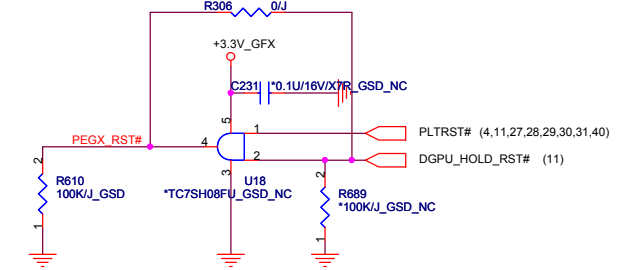
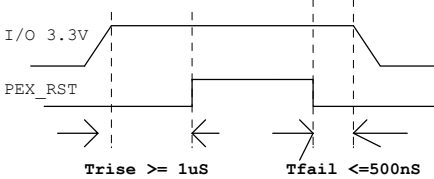
## power up sequence



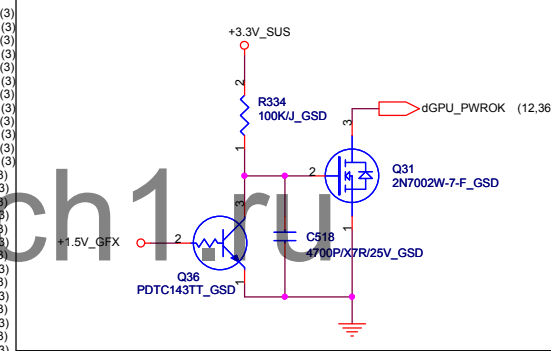
## NVVDD Maximum Settling Time



## PEX\_RST timing



## GPU all PWROK



PEX\_TSTCLK\_OUT/PEX\_TSTCLK\_OUT\_N  
DG-05093-001\_V02:Page 70  
default can be unstuffed  
Scott-0711

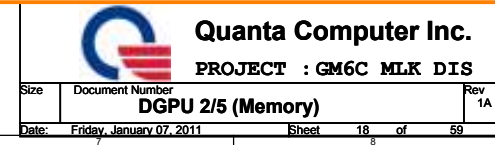
PEX\_CLKREQ\_N  
DG-05093-001\_V02:Page 70  
Pull down 2.49K/F  
Scott-0711

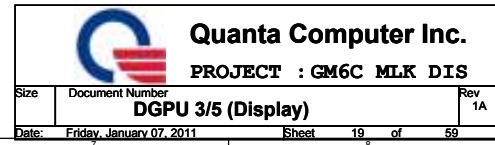
PEX\_TERM  
DG-05093-001\_V02:Page 70  
Pull down 10K  
Scott-0711

TESTMODE  
DG-05093-001\_V02:Page 207  
Pull down 10K  
Scott-0711

PEX\_PLIVDD  
DG-05093-001\_V02:Page 71,72  
120mA each  
Scott-0710

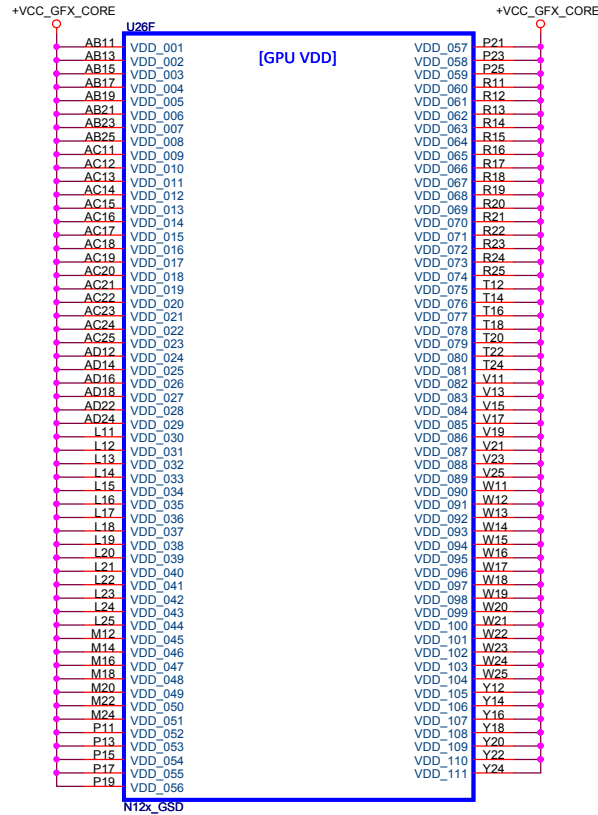
PEX\_CLKREQ# circute is different with GM6.  
Confirm with GM6



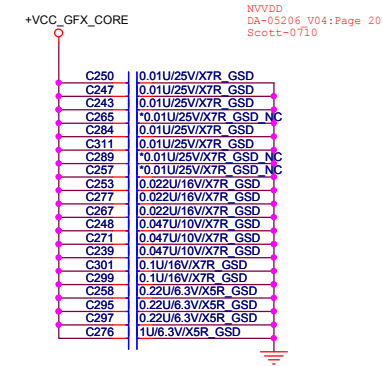




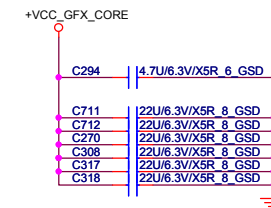
31.56A



# PLACE UNDER BALLS



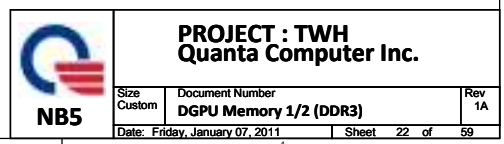
# PLACE NEAR BALLS



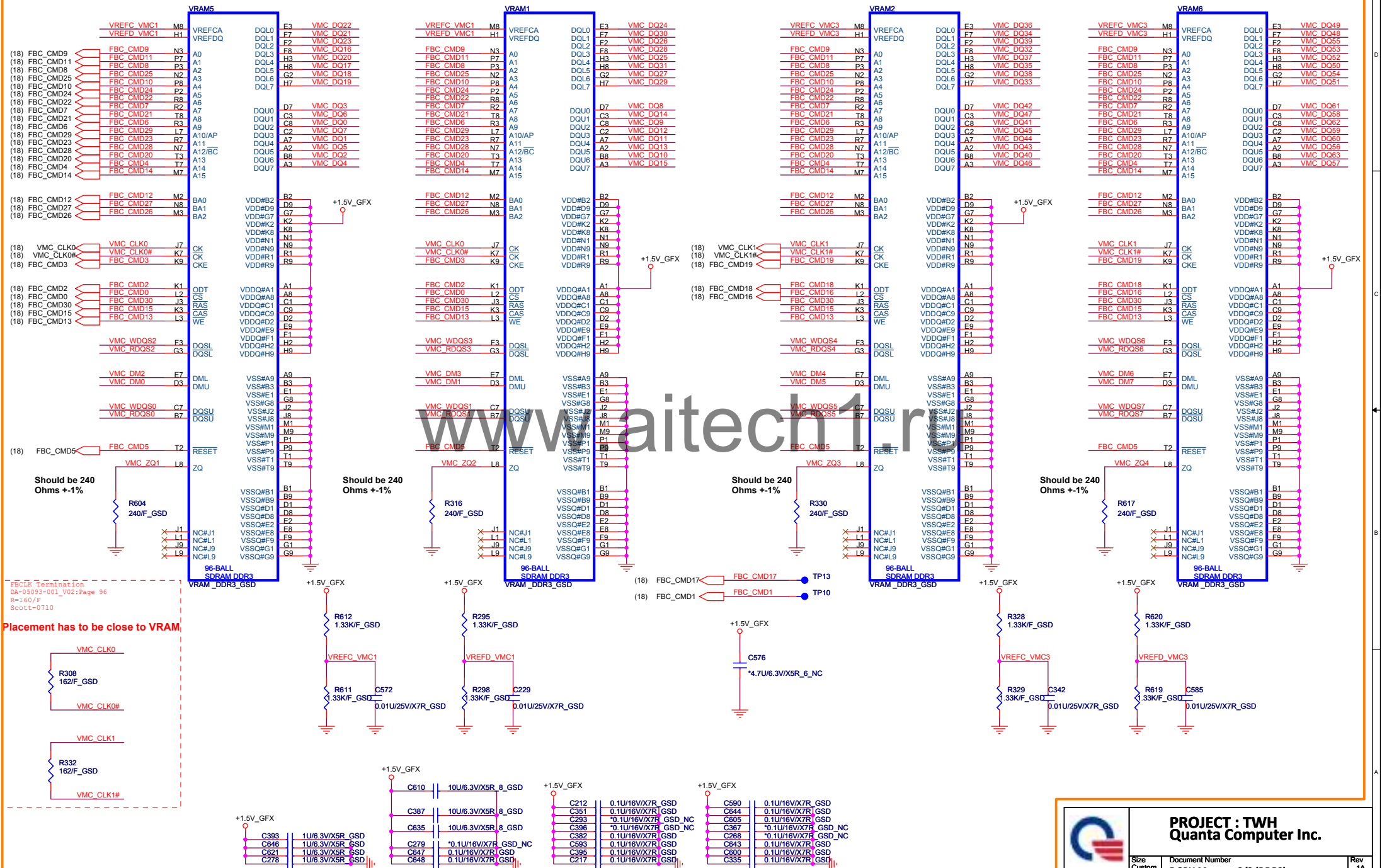
Quanta Computer Inc.

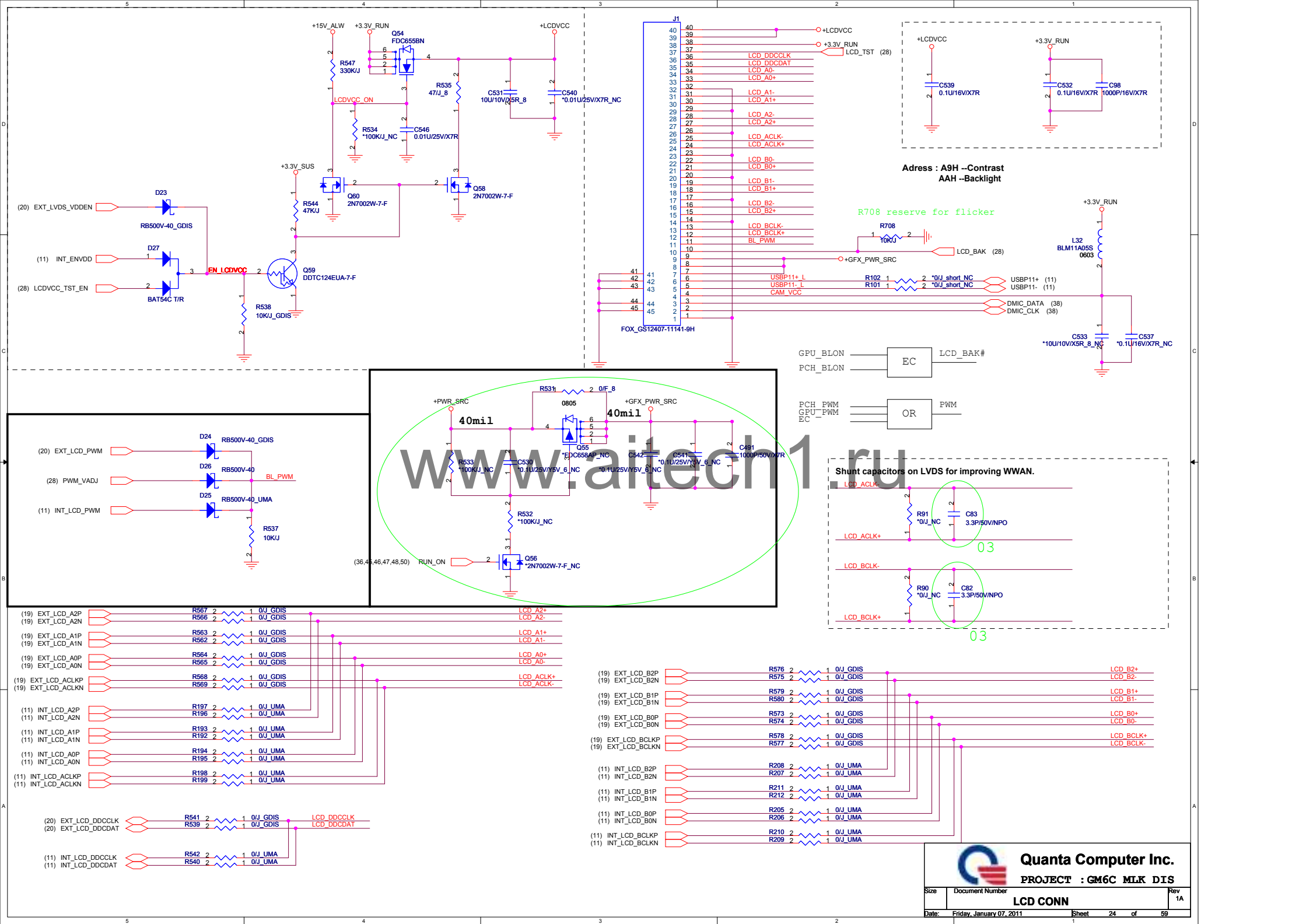
PROJECT : GM6C MLK DIS

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	DGPU 5/5 (Power/Ground)	1A
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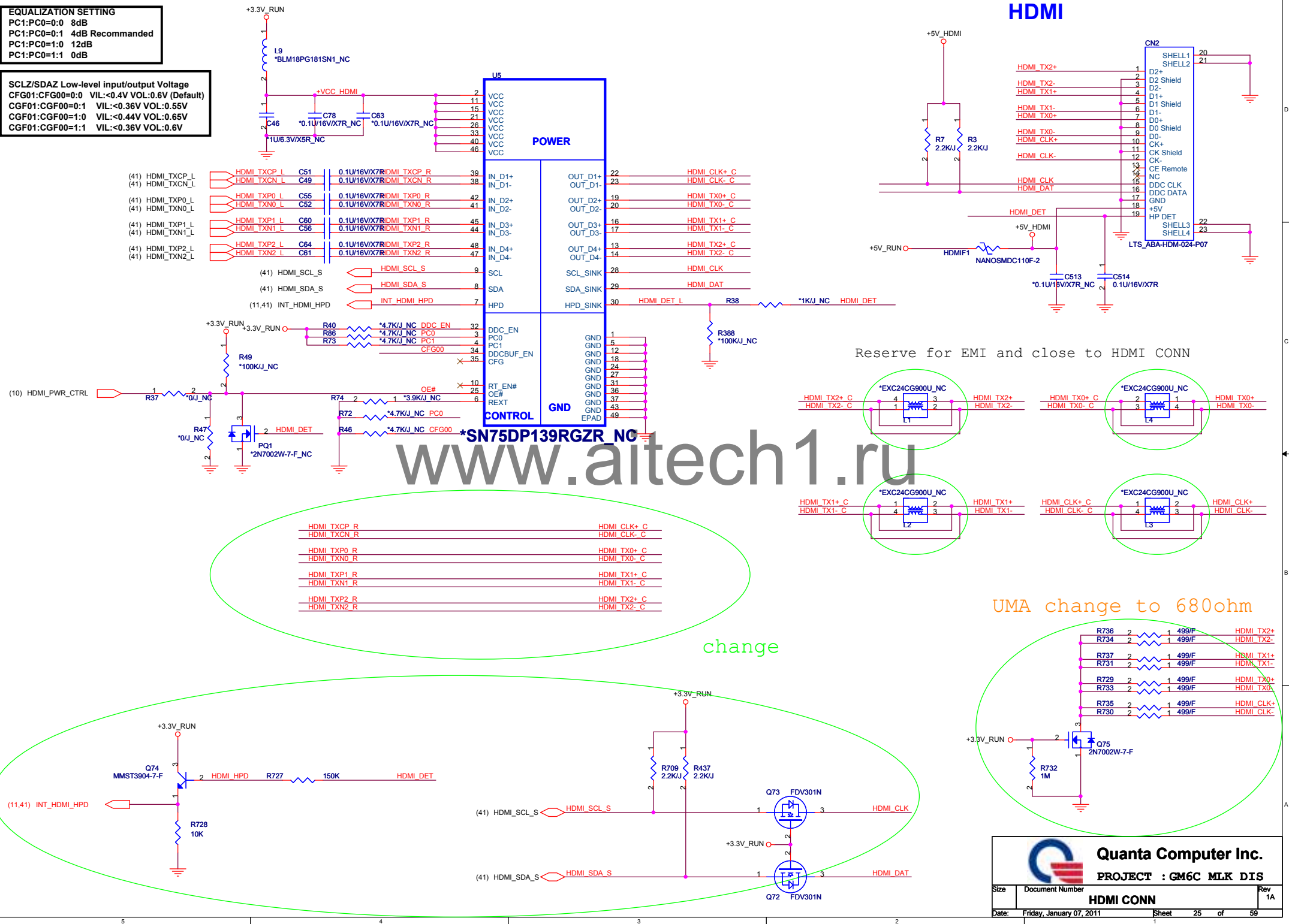
**CHANNEL B: 256MB/512MB DDR3**



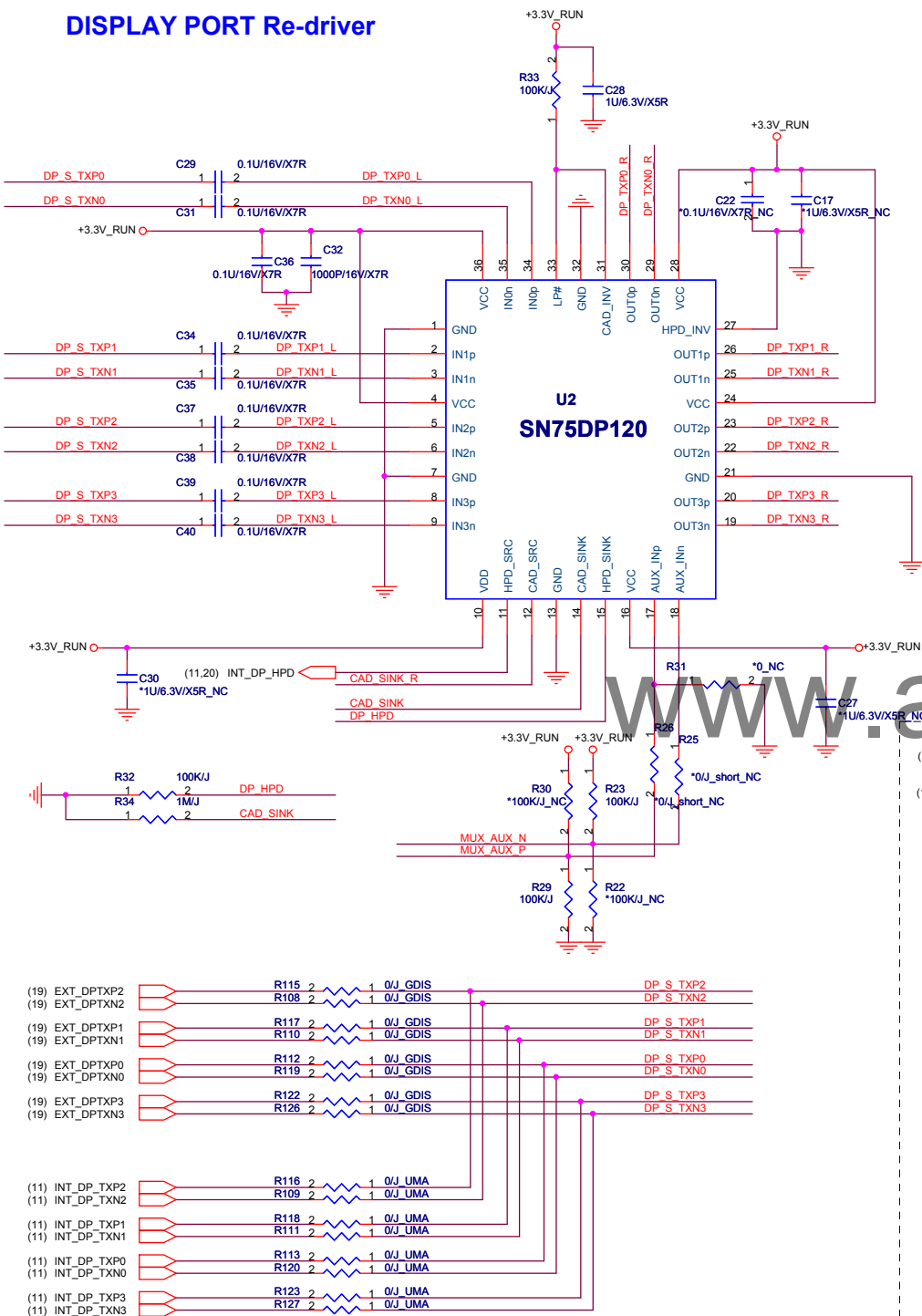


**EQUALIZATION SETTING**  
 PC1:PC0=0:0 8dB  
 PC1:PC0=0:1 4dB Recommended  
 PC1:PC0=1:0 12dB  
 PC1:PC0=1:1 0dB

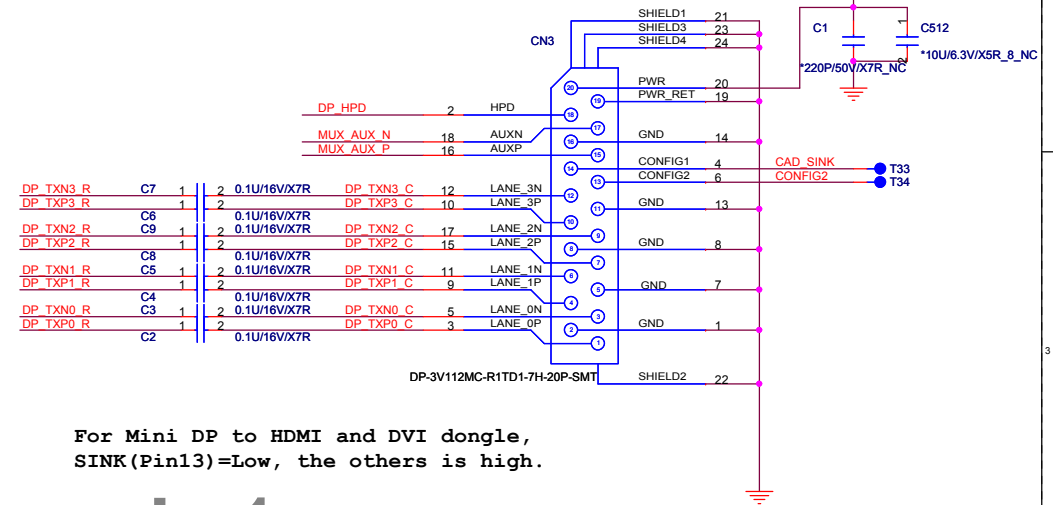
**SCLZ/SDAZ Low-level input/output Voltage**  
 CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)  
 CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V  
 CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V  
 CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V



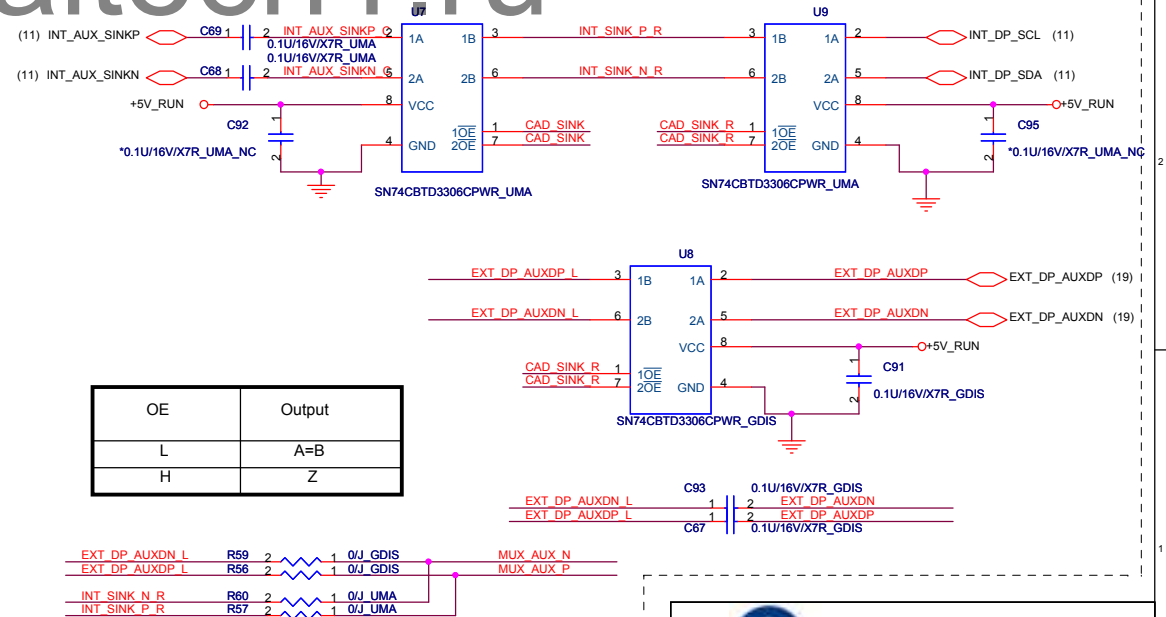
## DISPLAY PORT Re-driver



## MINI DISPLAY PORT CONNECTOR



For Mini DP to HDMI and DVI dongle,  
SINK(Pin13)=Low, the others is high.



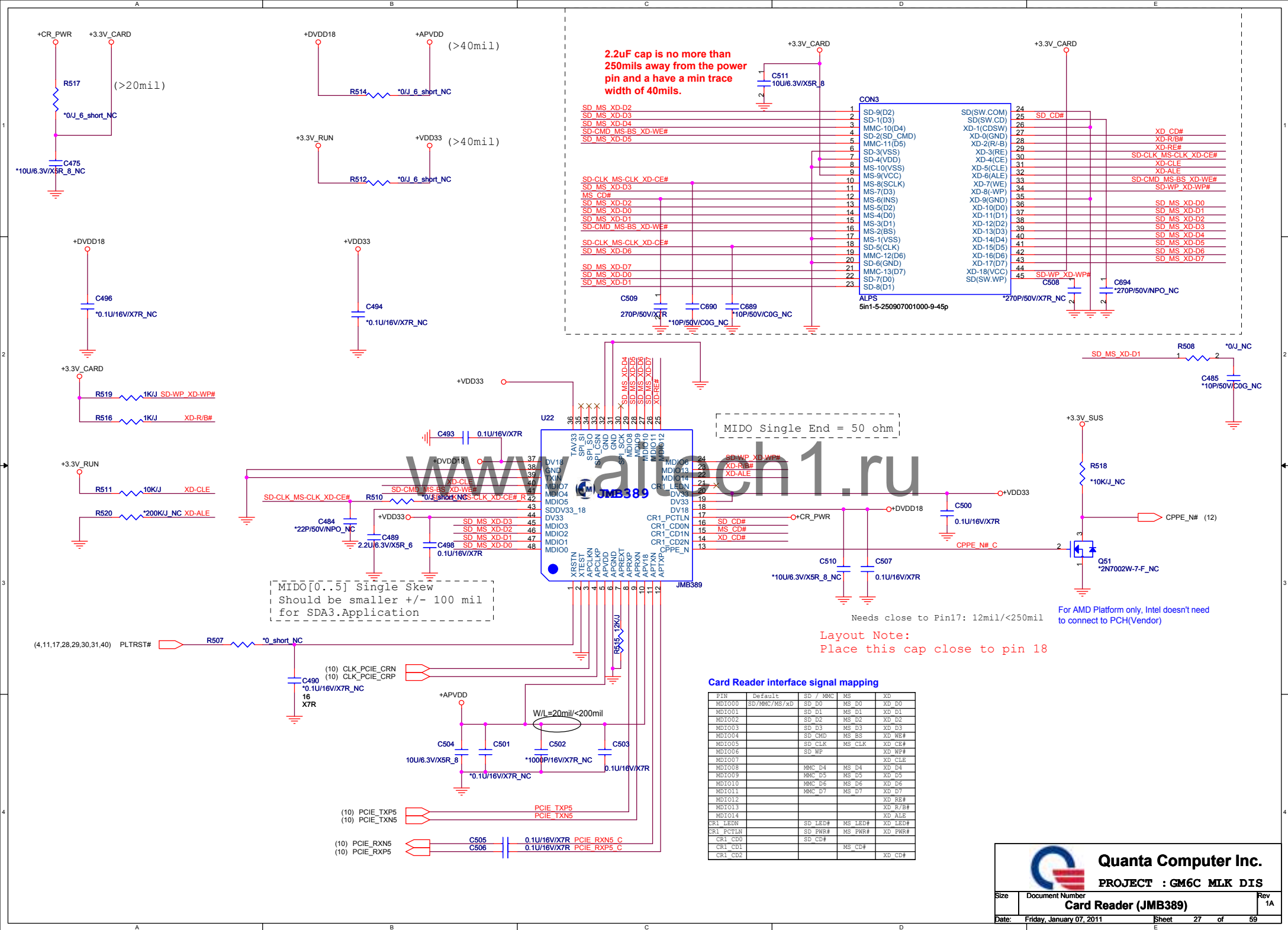
OE	Output
L	A=B
H	Z

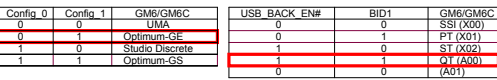
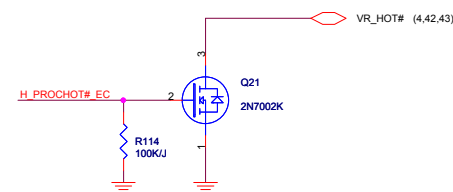
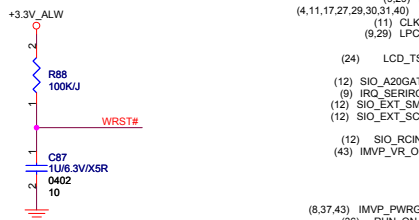
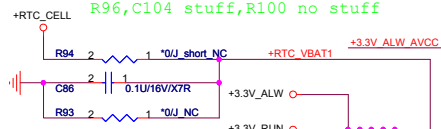


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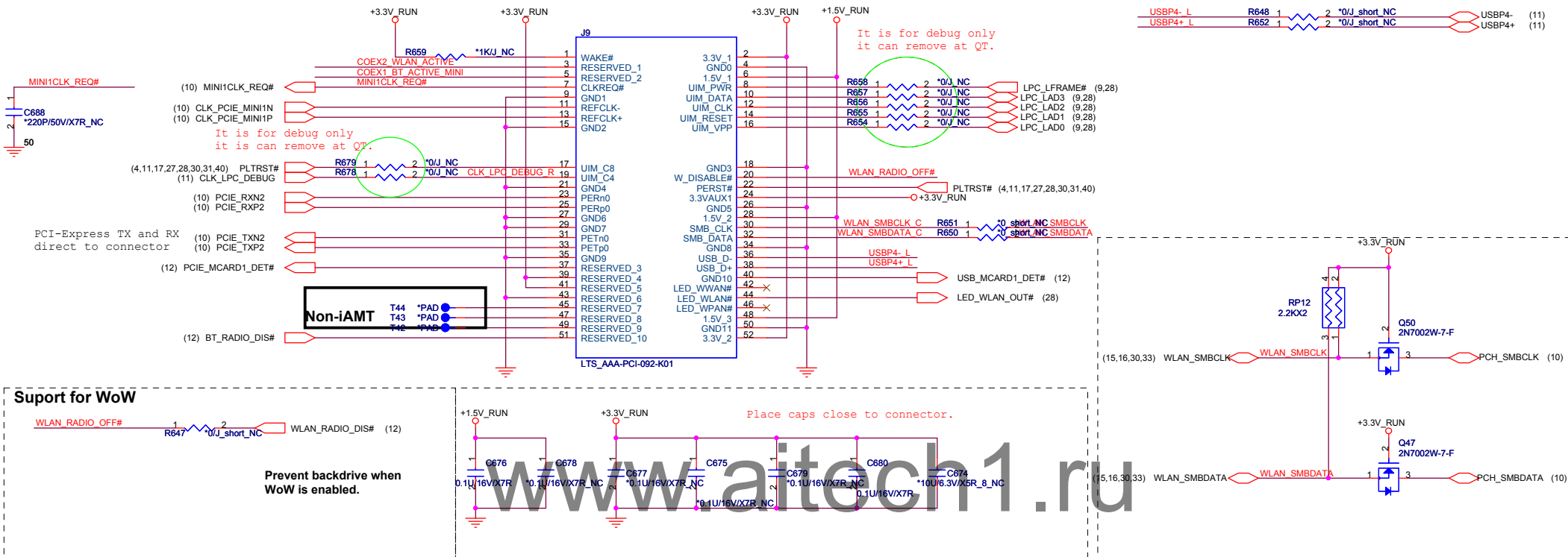
PROJECT : GM6C MLK DIS

MINI DP CONN

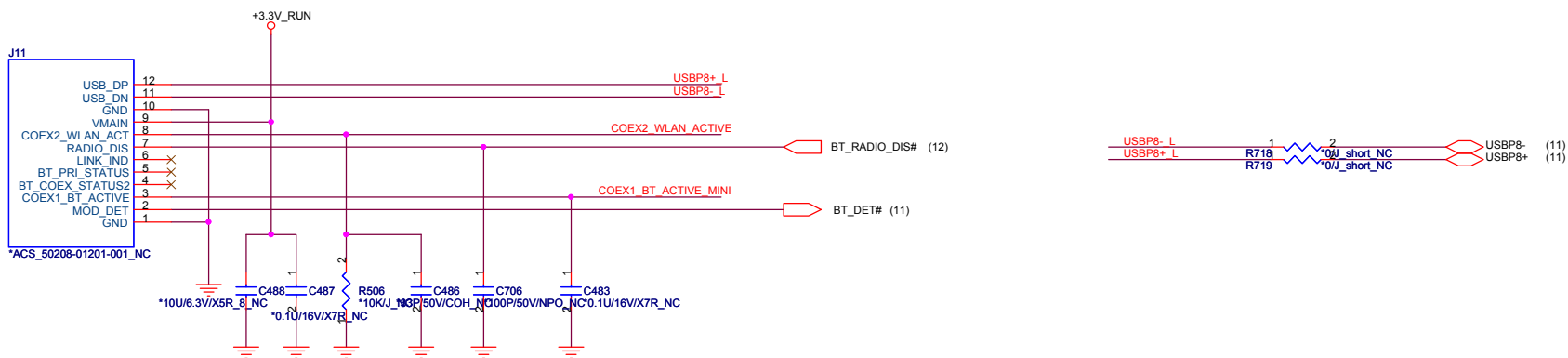




## MiniCard WLAN connector



## Support Dell BT375 (Little Stone) module (XPS) W TO B

**Quanta Computer Inc.**

PROJECT : GM6C MLK DIS

### MINI-Card (WLAN/WPAN)

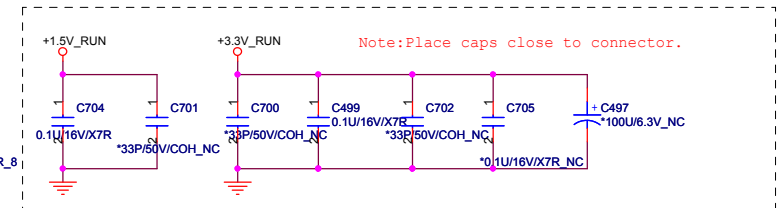
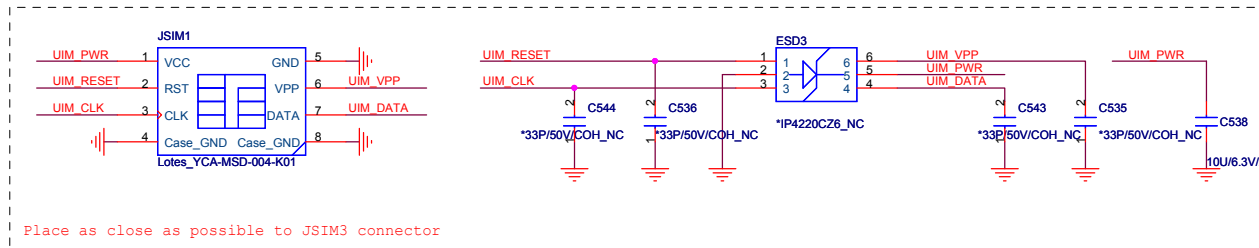
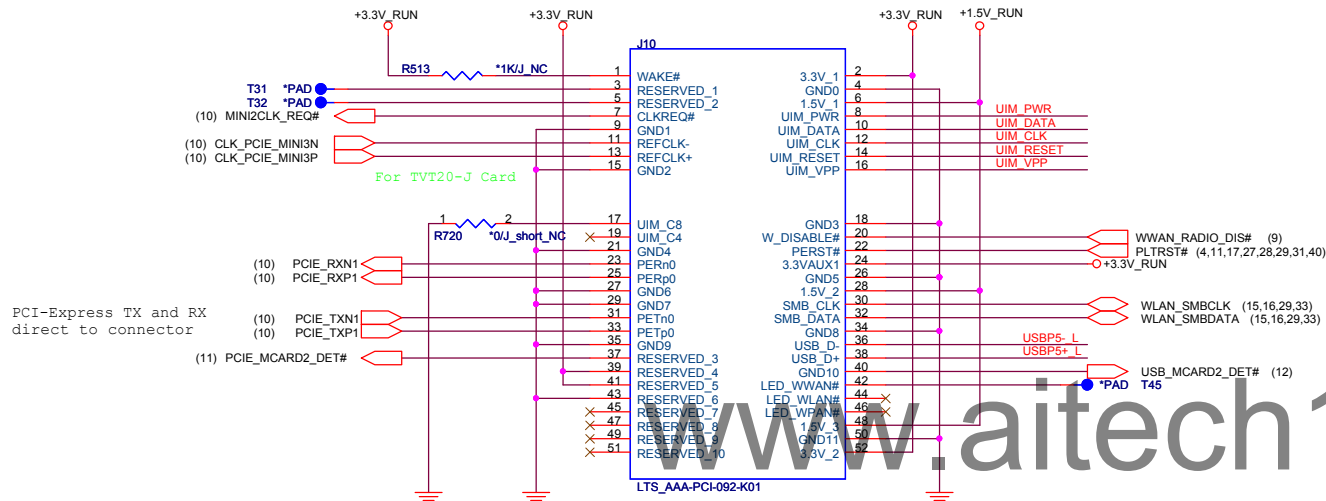
Size	Document Number
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		<b>MINI-CASE</b>
--	--	------------------

**LAN/WPAN)**

	R
--	---

## MiniCard WWAN connector



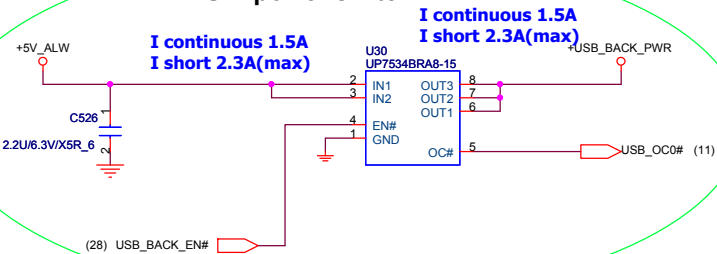
**Quanta Computer Inc.**

**PROJECT : GM6C MLK DIS**

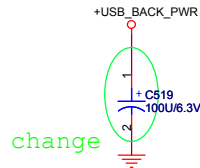


# ESATA + USB Conn + Power Share

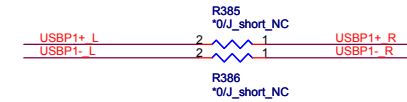
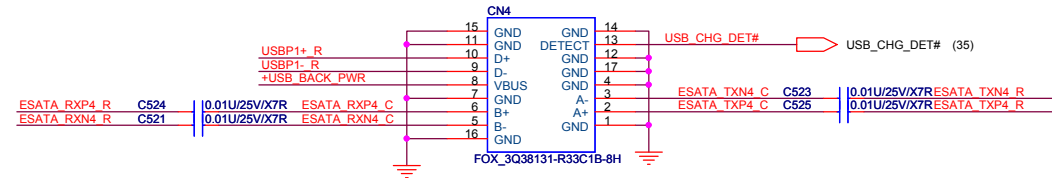
## UPI power switch



USB\_BACK\_EN# needs to be low when system S3 and S5 for USB charge



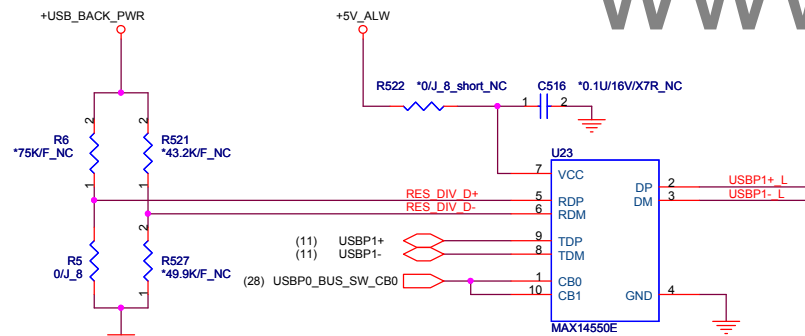
This pin connects to 3VALW ON POWER LOGIC



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## E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB

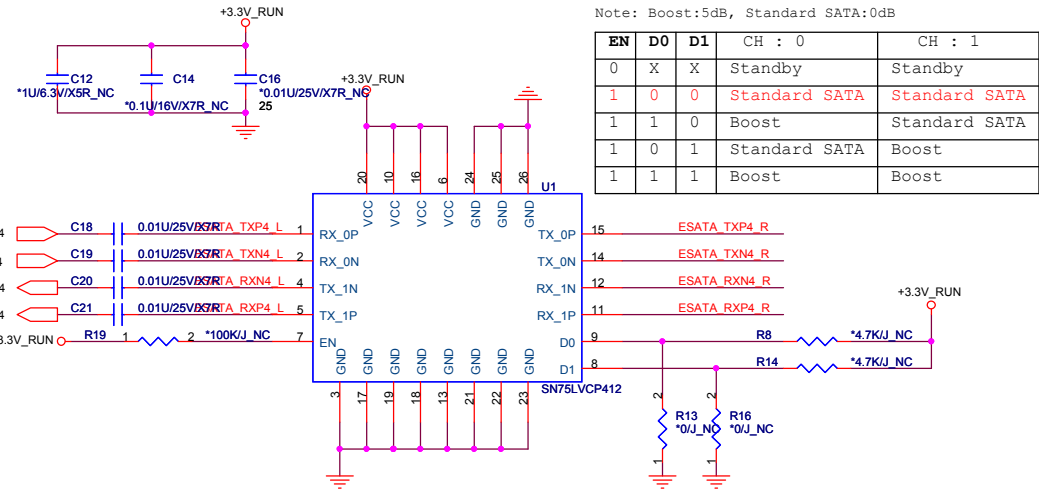


EC needs to drive CB0/CB1 pins to low when system S3/S5 and drive high when system S0.

U49 PN and Footprint needs to double check

R15 needs to be 49.9K\_F if we use external resistors.

CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only
(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)		
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)		



Note: Boost:5dB, Standard SATA:0dB

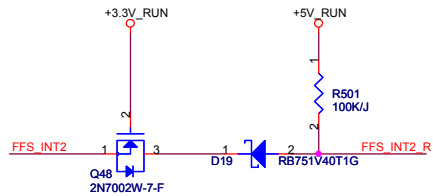
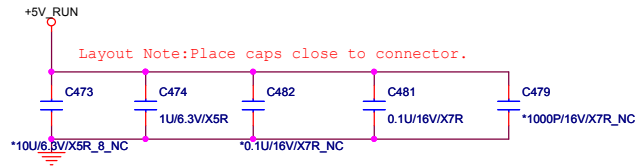
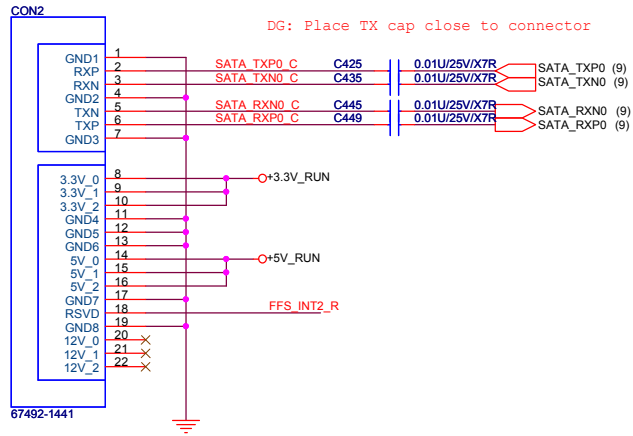
EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



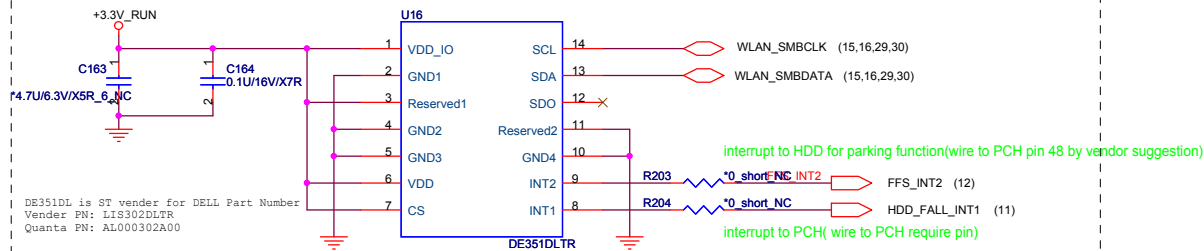
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PROJECT : GM6C MLK DIS

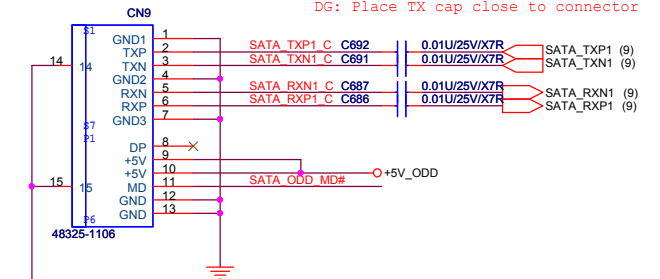
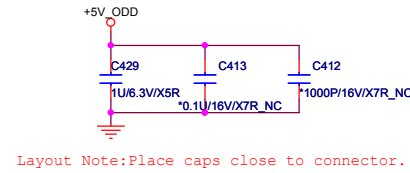
## SATA Connector.



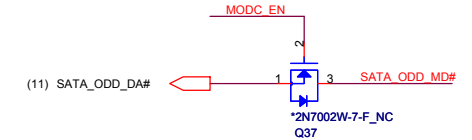
## 3-axis Fall Sensor (HDD data protector)



## ODD Connector



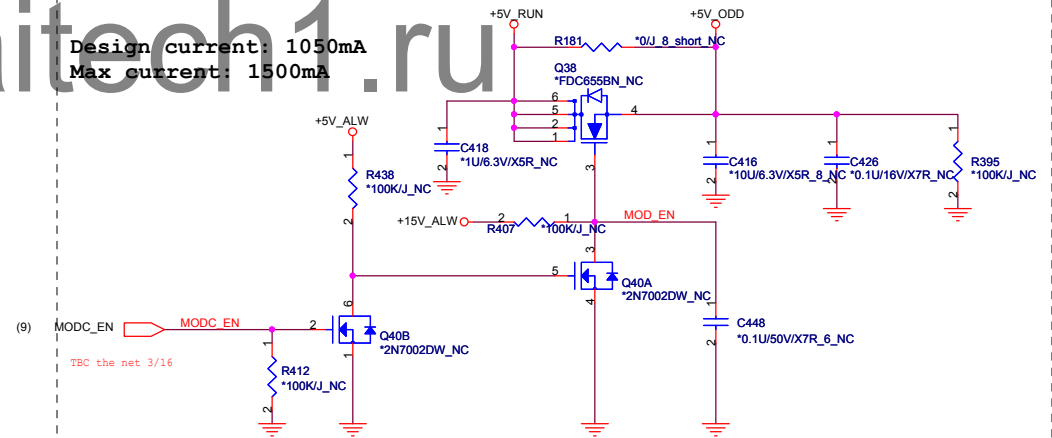
## Backwards Compatibility



Drive powered on, MD# is High  
Drive powered off, MD# is Low

Because the drive does not support ZPODD, the driver never powers off the power FET and never connects the MD/DA pin to the drive

Design current: 1050mA  
Max current: 1500mA



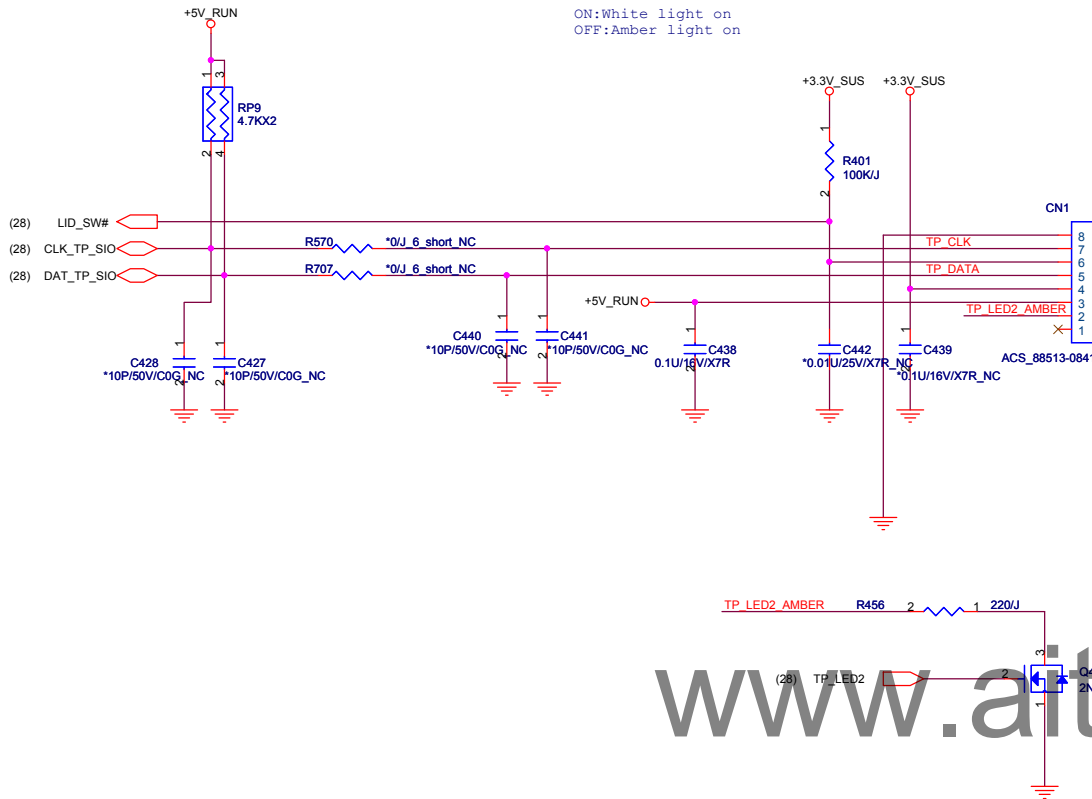
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

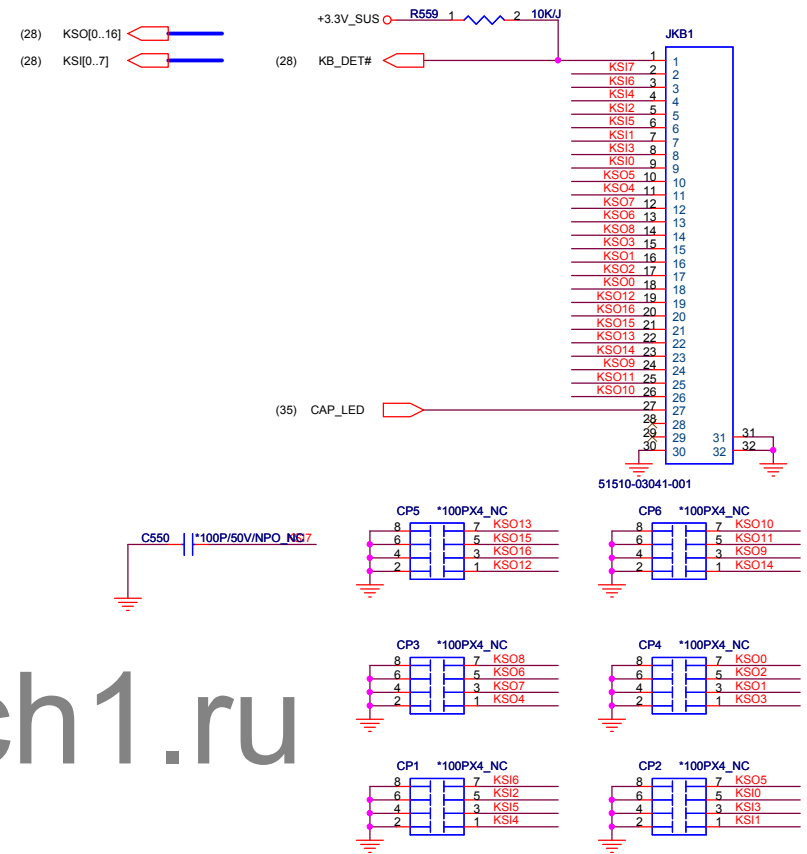
SATA (HDD&ODD)

## Touch Pad

ON:White light on  
OFF:Amber light on

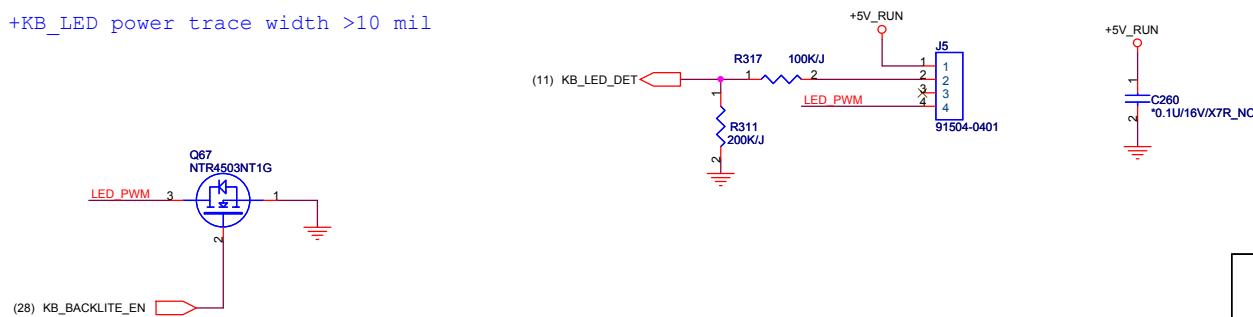


## KEYBOARD CONNECTOR



## Key board illumination

+KB\_LED power trace width >10 mil

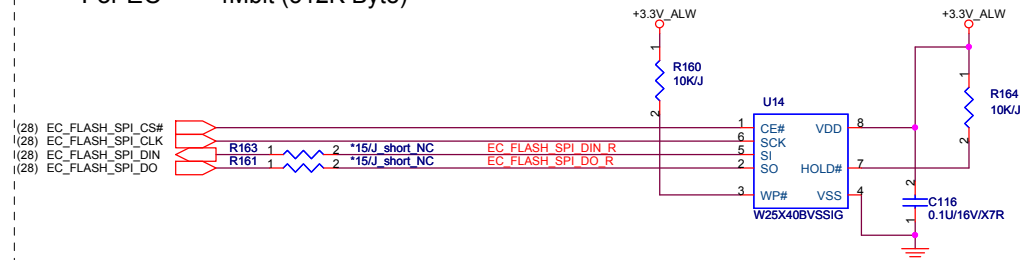


**Quanta Computer Inc.**

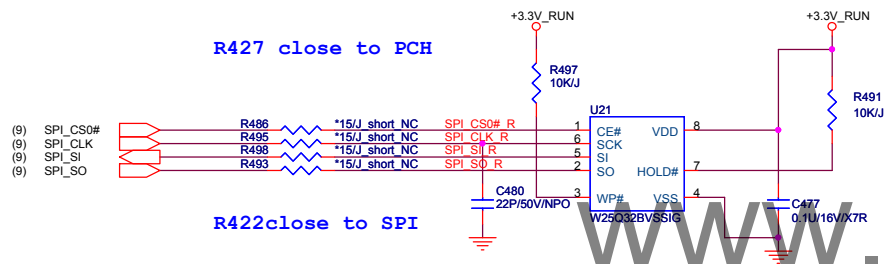
**PROJECT : GM6C MLK DIS**



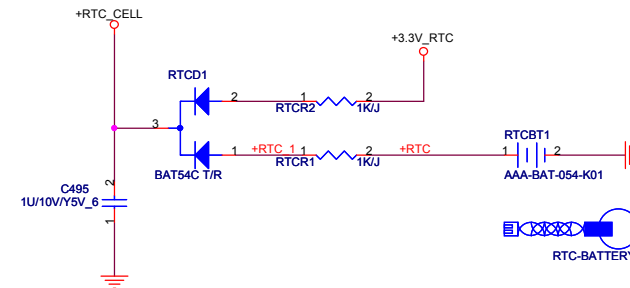
## For EC 4Mbit (512K Byte)



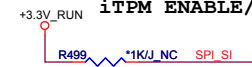
## For PCH 32Mbit (4M Byte)



## RTC BATTERY



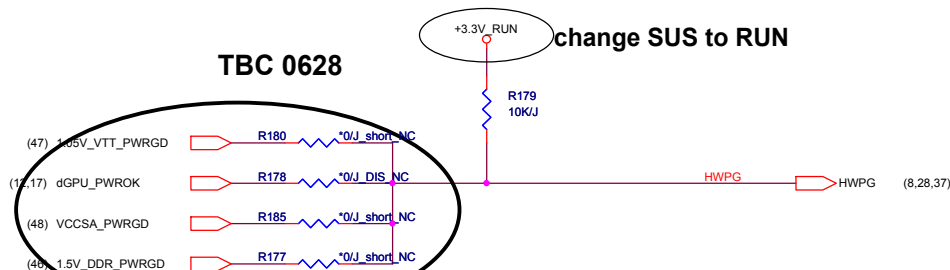
## iTPM ENABLE/DISABLE



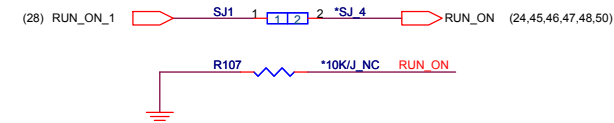
TPM Function	R428
Enable	Mount
Disable	NC (Default)

## RESET CIRCUIT

### TBC 0628

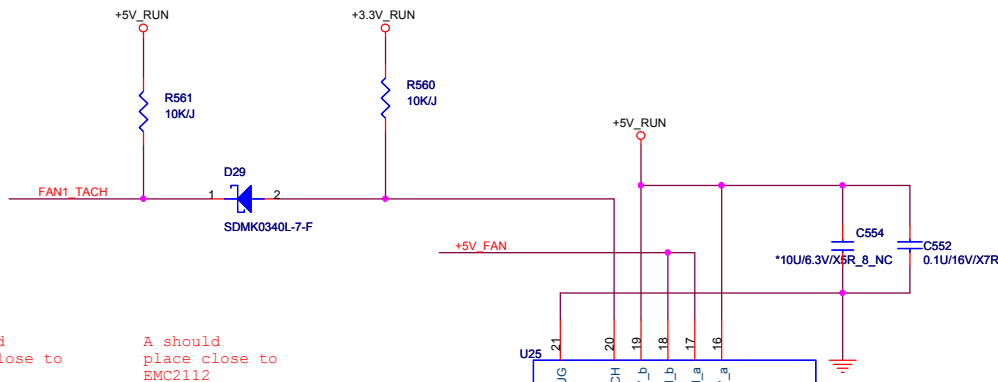
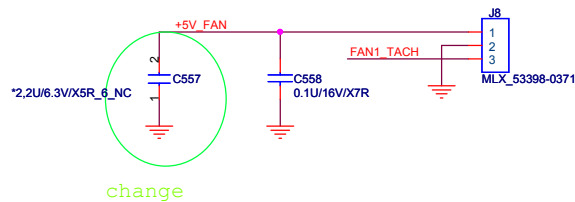


delet VTT\_POWERGOOD(07/12)



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PROJECT : GM6C MLK DIS



Need to check with BIOS

ADDR\_SEL

HIGH: 0101 110xb

OPN: 0111 101xb

GND: 0101 111xb

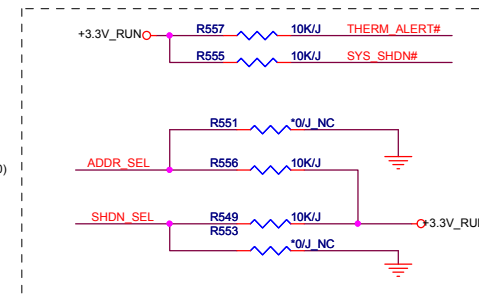
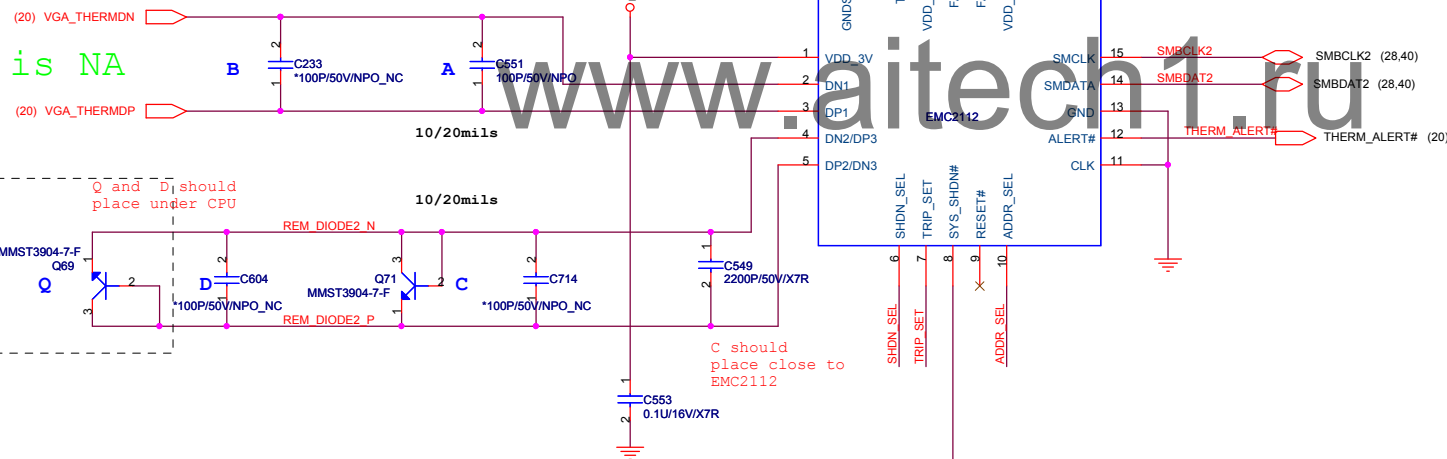
SHDN\_SEL

HIGH: External Diode 2 Mode

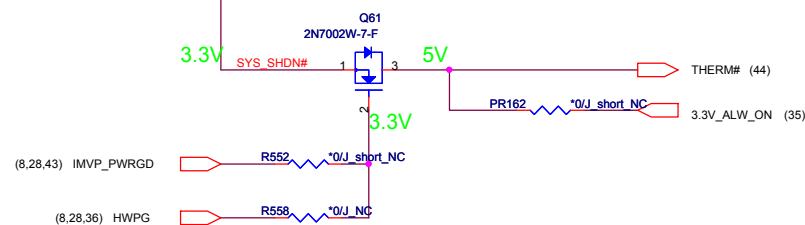
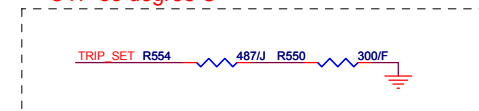
OPN: AMD CPU/Diode Mode

GND: Intel Transistor Mode

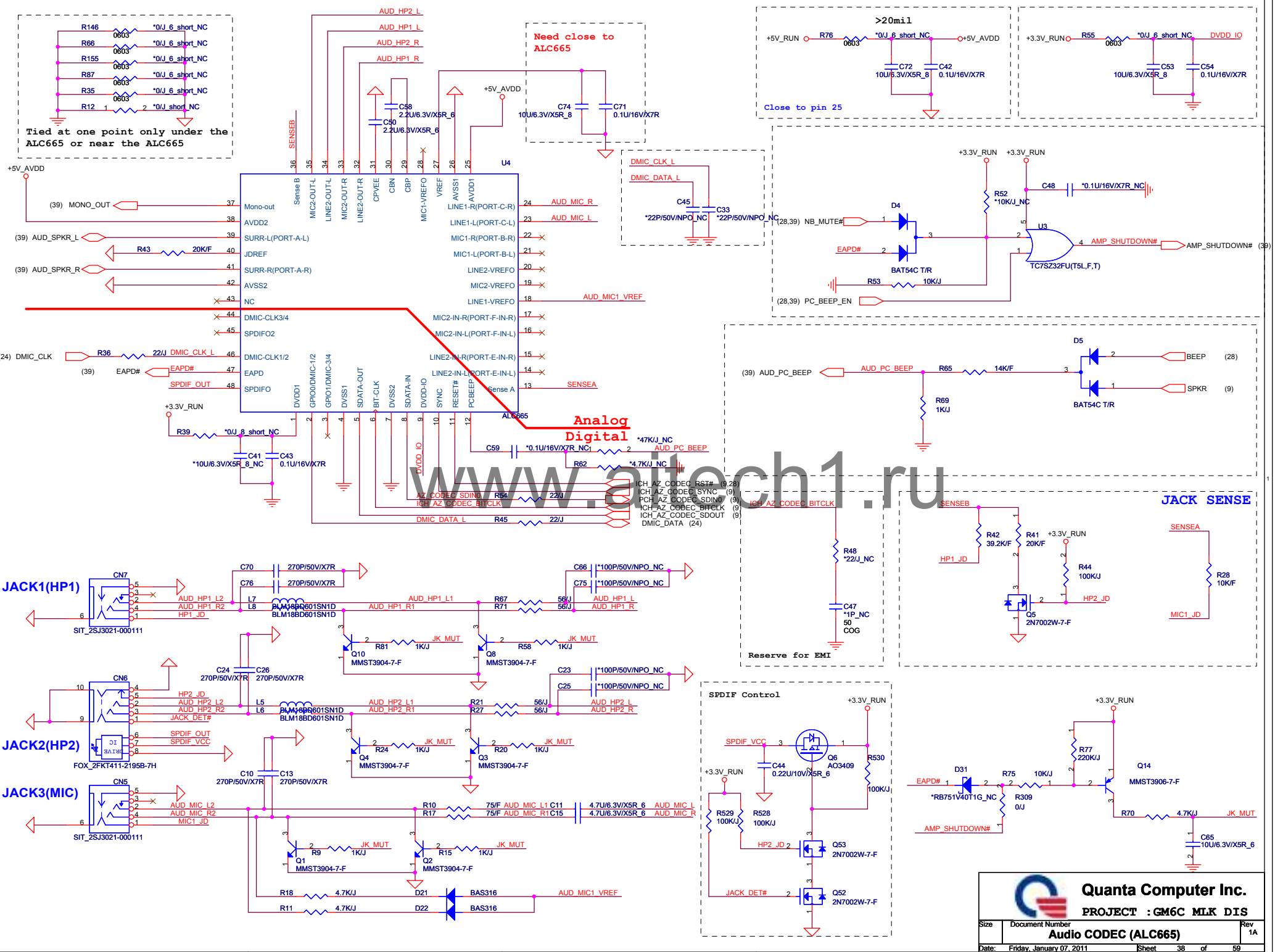
B should place close to GFX  
A should place close to EMC2112



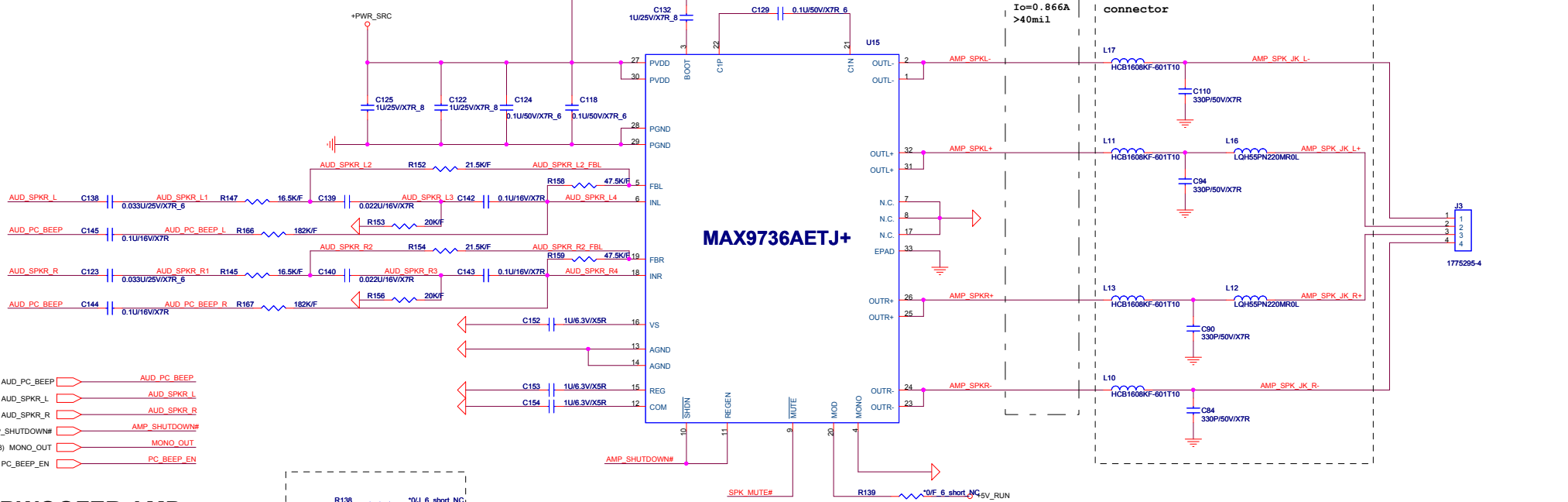
OTP 85 degree C



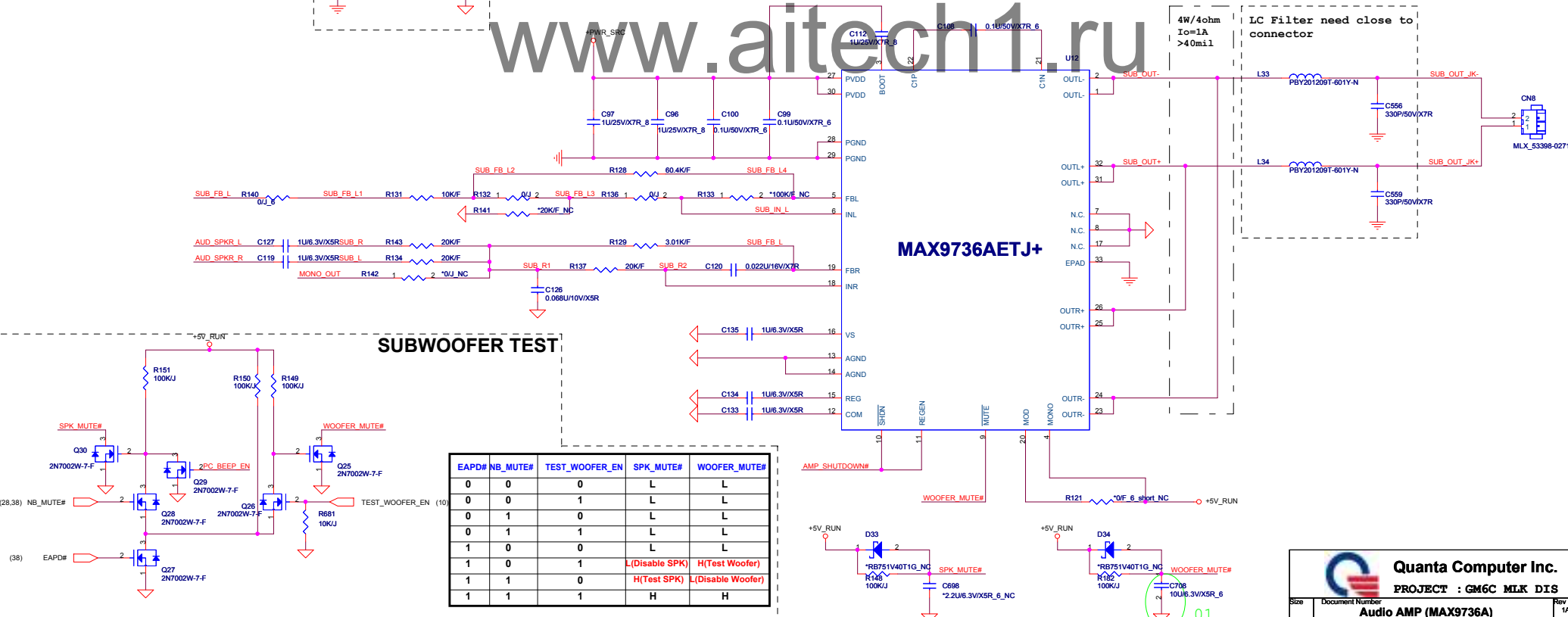
reserve HWPG only HW control (07/12)



Main Speaker AMP

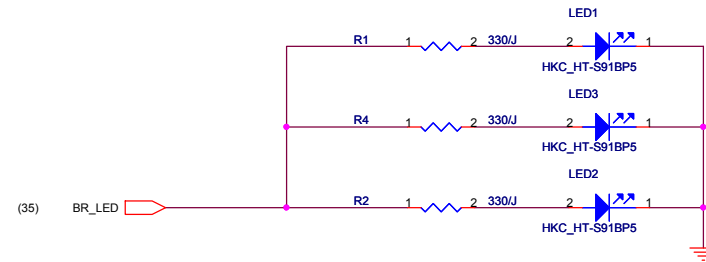
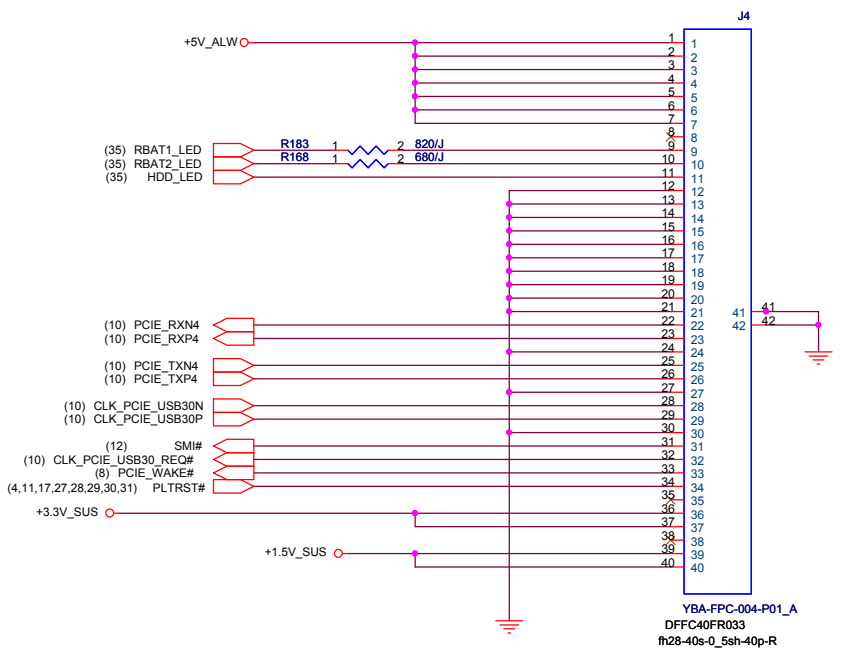


SUBWOOFER AMP

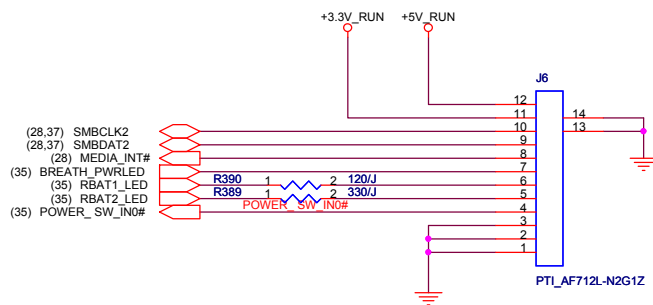


SUBWOOFER TEST

EAPD#	NB_MUTE#	TEST_WOOFER_EN	SPK_MUTE#	WOOFER_MUTE#
0	0	0	L	L
0	0	1	L	L
0	1	0	L	L
0	1	1	L	L
1	0	0	L	L
1	0	1	L(Disable SPK)	H(Test Woofer)
1	1	0	H(Test SPK)	L(Disable Woofer)
1	1	1	H	H



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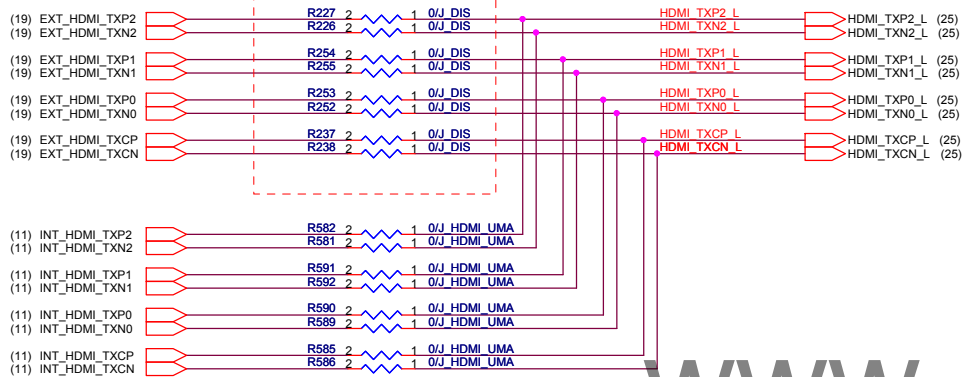
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PROJECT : GM6C MLK DIS

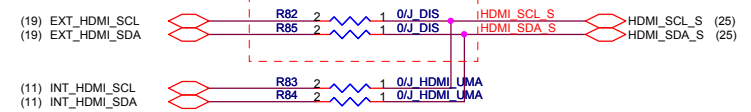
Size	Document Number	Rev
	Left USB/MMB CONN	1A
Date:	Friday, January 07, 2011	Sheet 40 of 59

## HDMI Switch

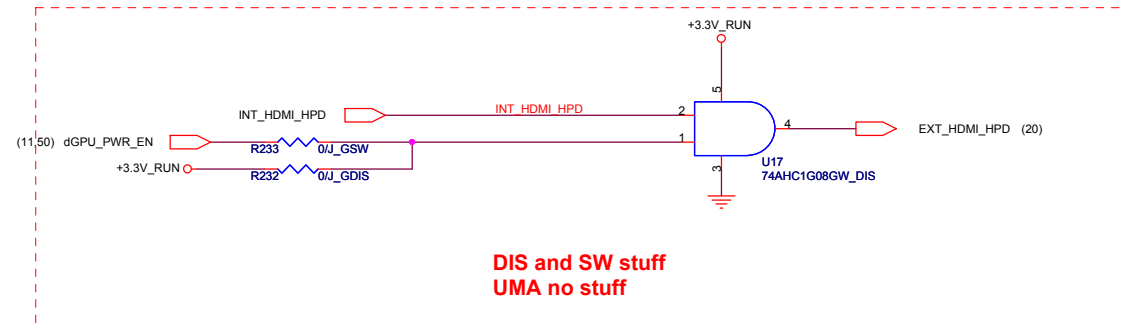
DIS and SW stuff  
UMA no stuff



DIS and SW stuff  
UMA no stuff



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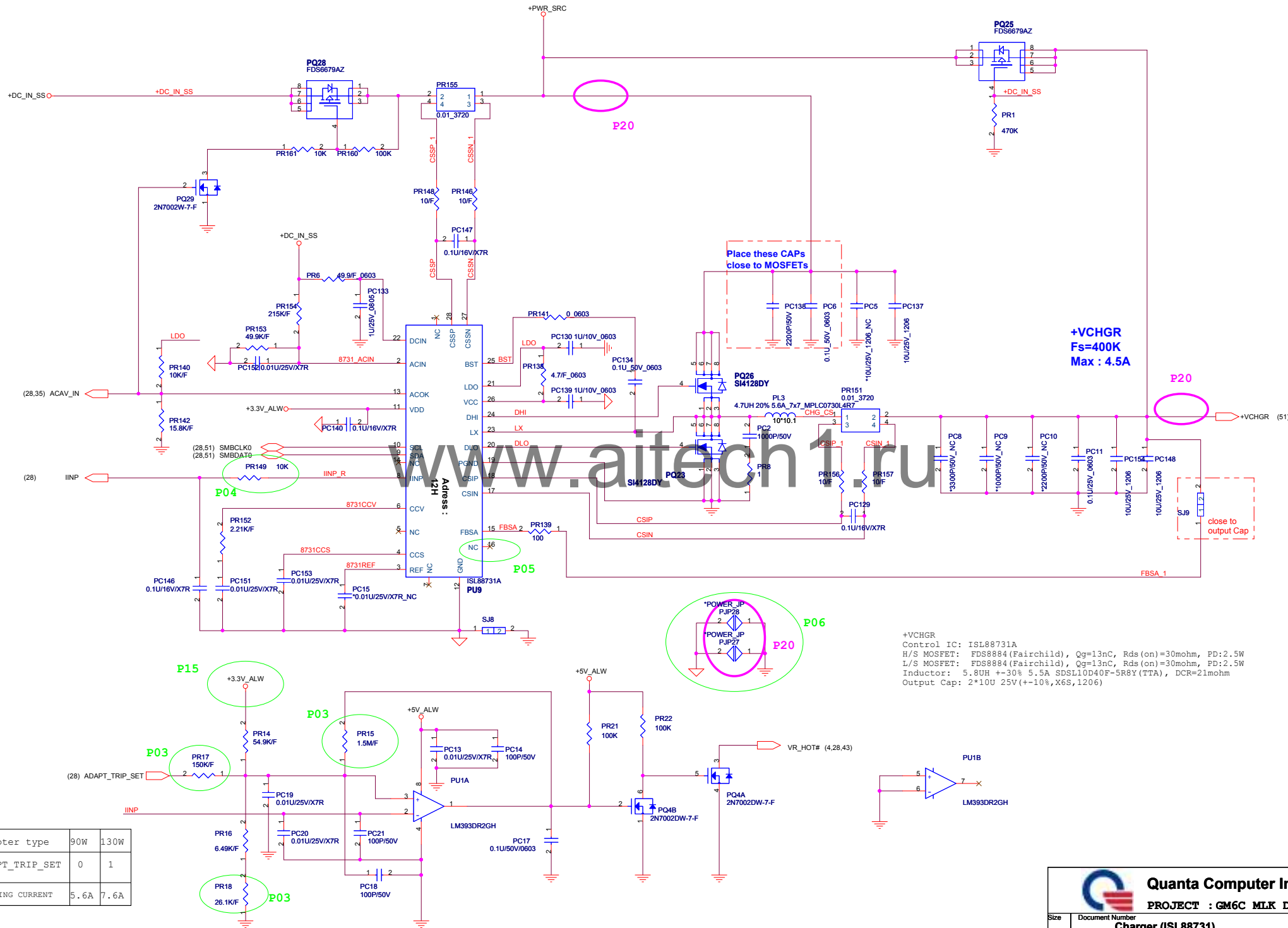
DIS and SW stuff  
UMA no stuff



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PROJECT : GM6C MLK DIS

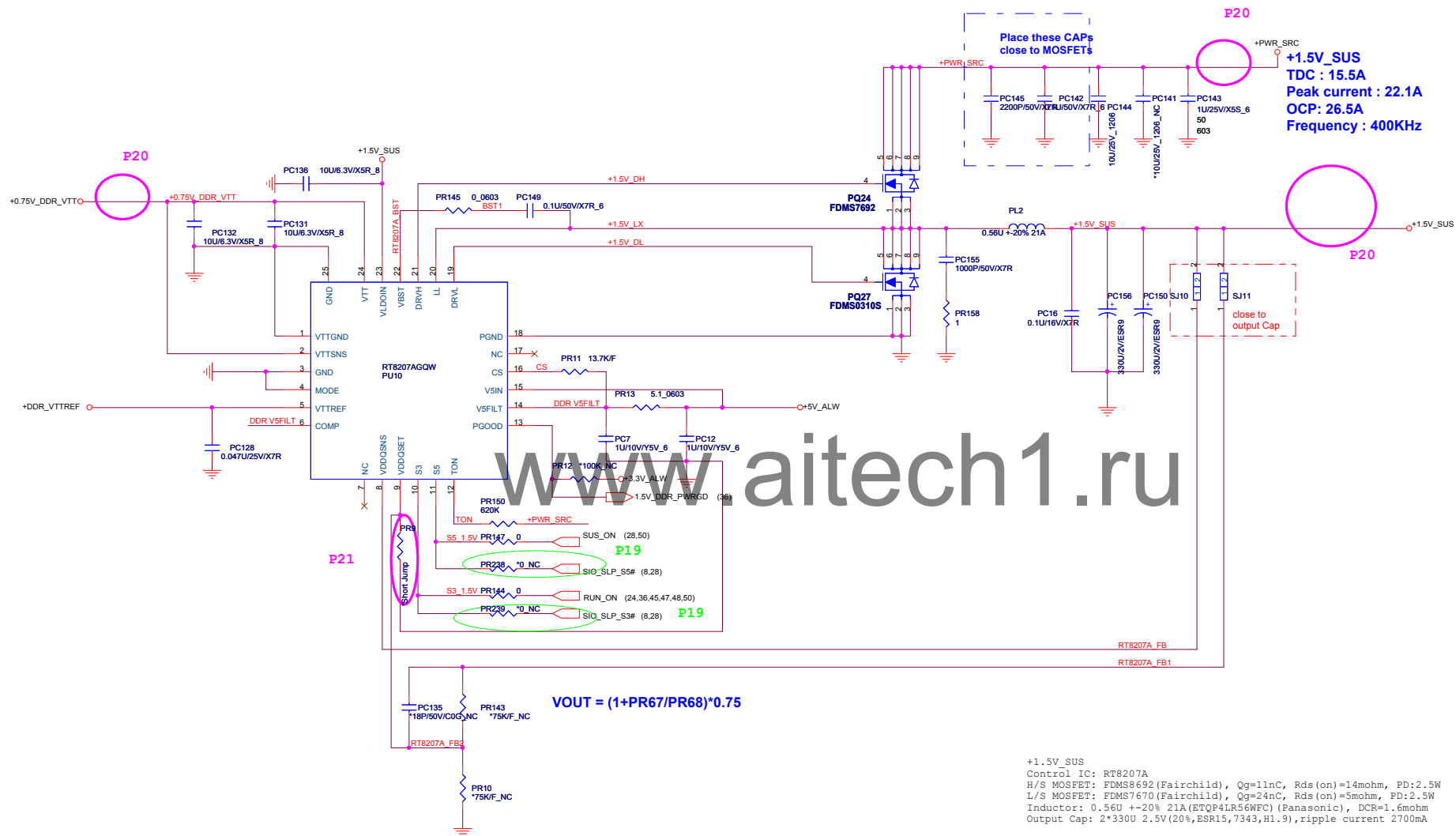
Size	Document Number	Rev
	BLANK	1A
Date:	Friday, January 07, 2011	Sheet 41 of 59











VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

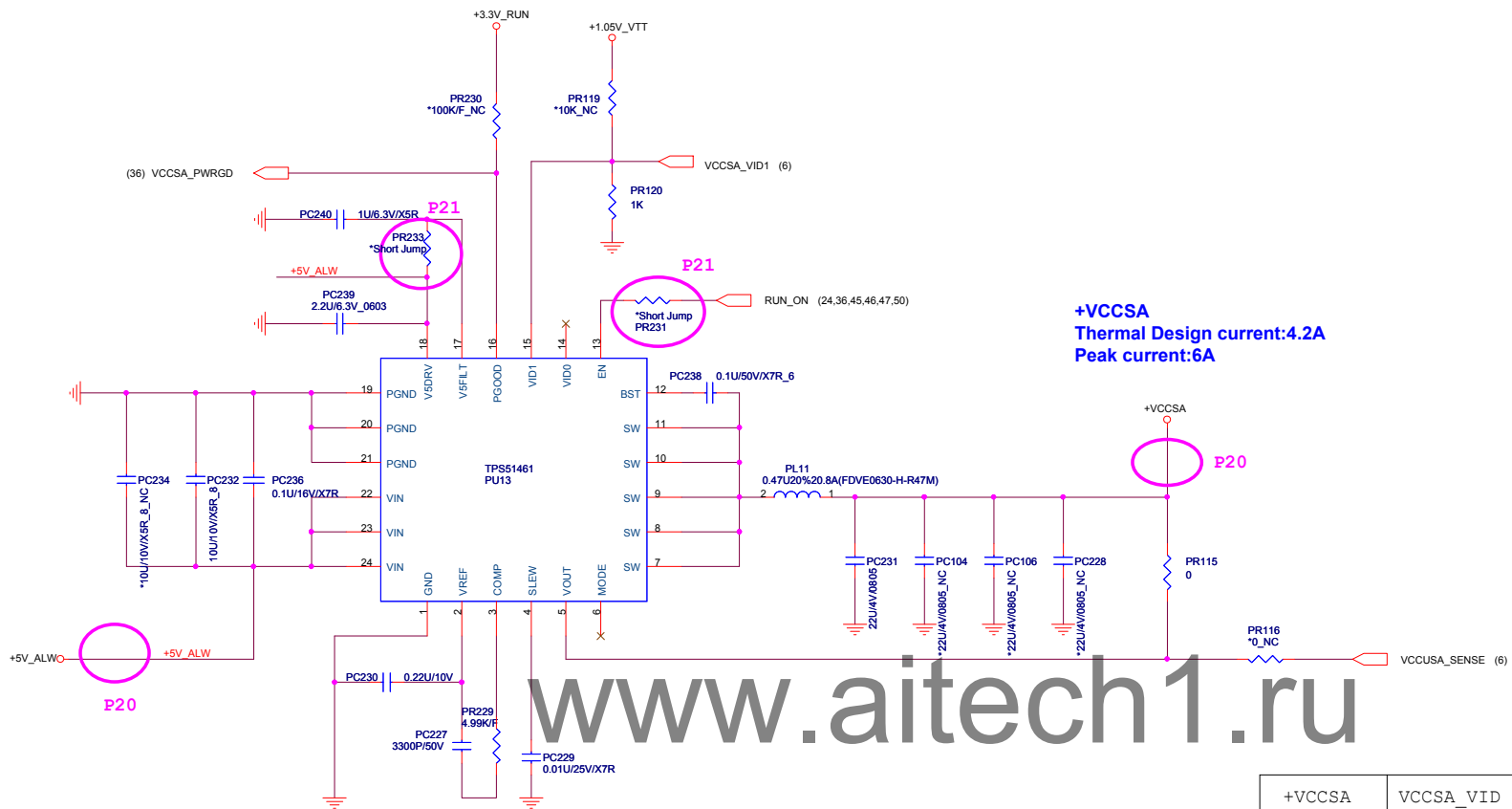
VDDQ output voltage selection

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)





**+VCCSA**  
Thermal Design current:4.2A  
Peak current:6A

+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low

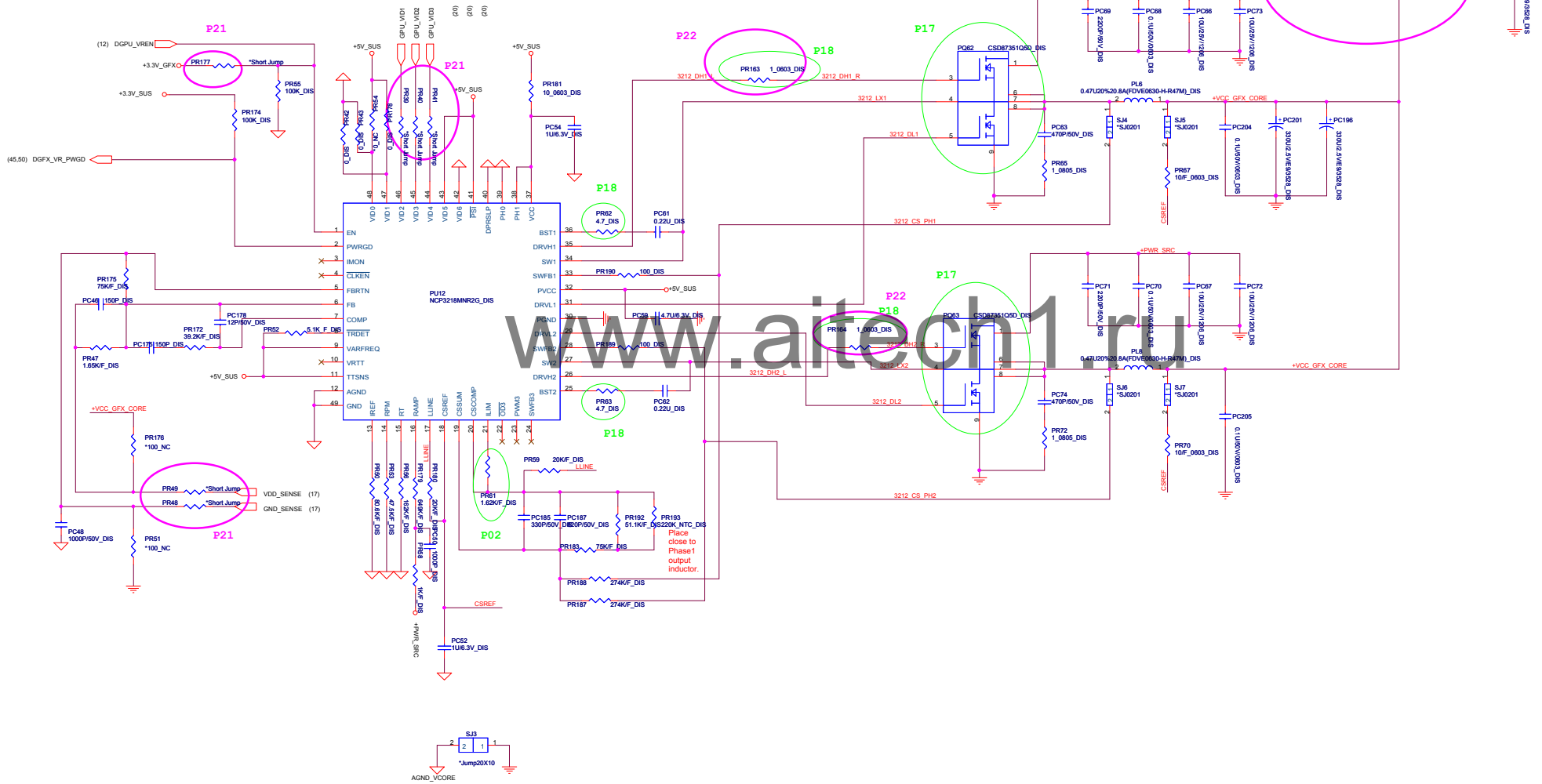
N12P-GE:

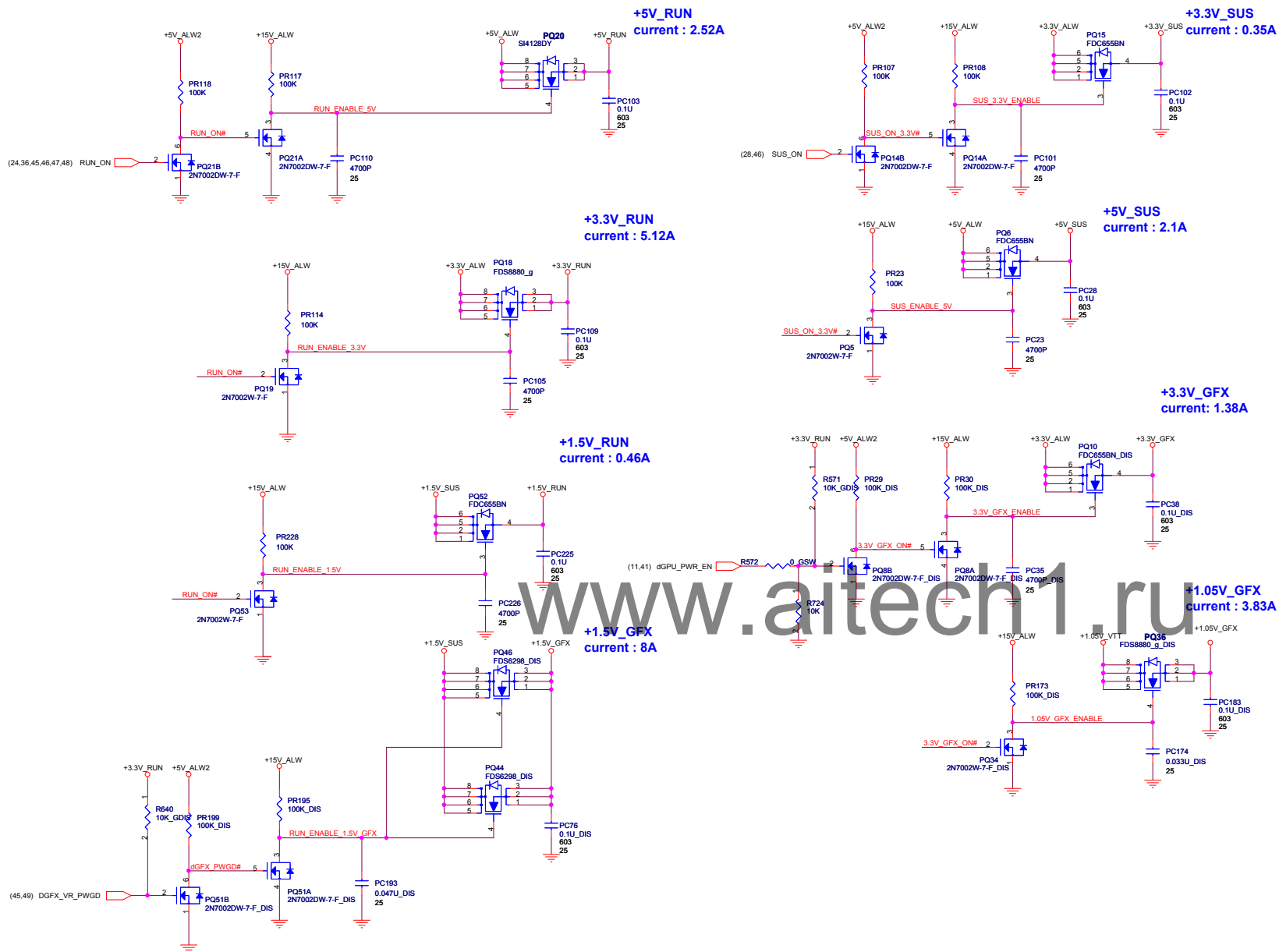
GPU VID3	GPU VID2	GPU VID1
0.85V	1	0
0.95V	0	1
1.0V	0	1

N12P-GS:

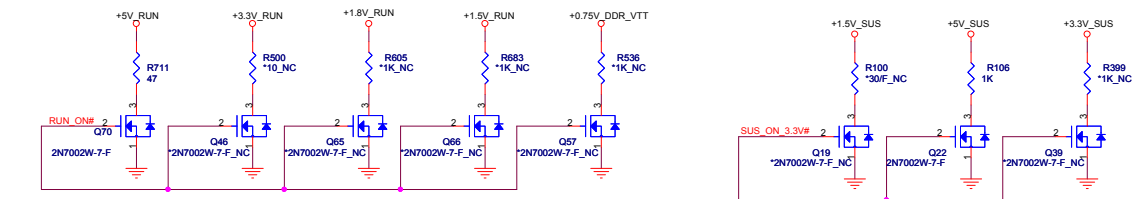
GPU VID3	GPU VID2	GPU VID1
0.825V	1	0
0.975V	0	1
1.0V	0	1

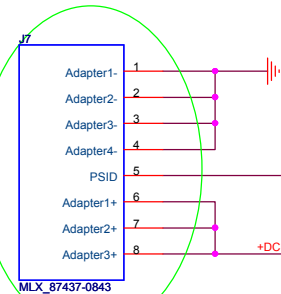
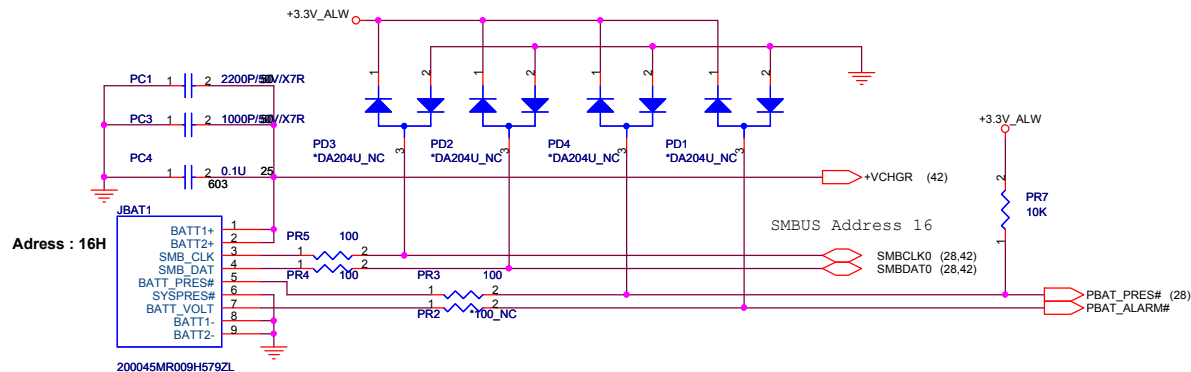
	N12P-GS	N12P-GE
PR42	NC	0_DIS
PR178	0_DIS	NC



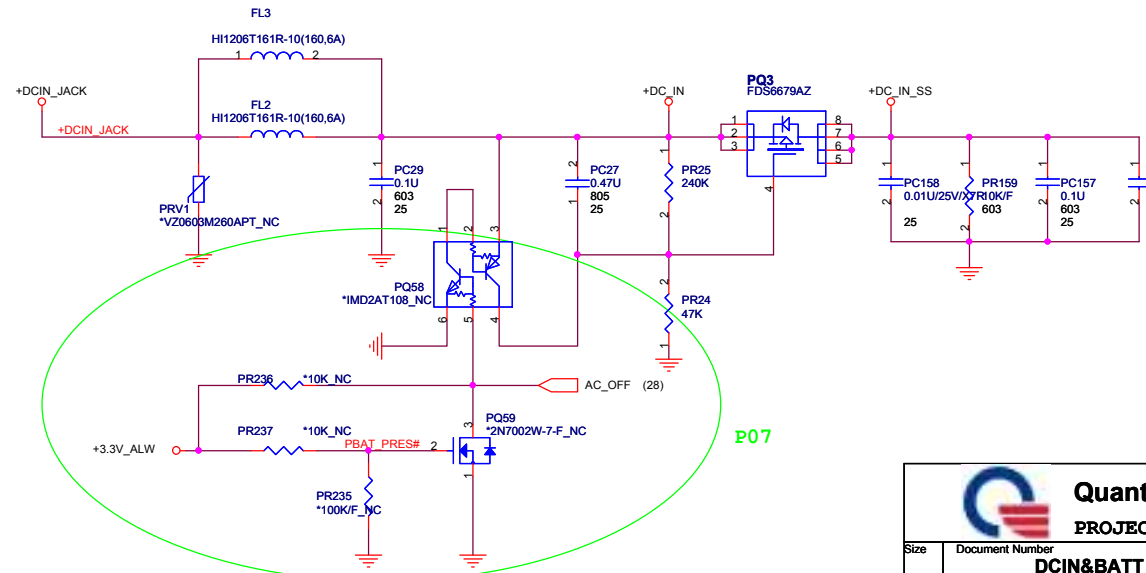
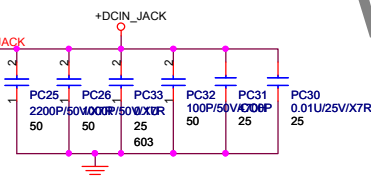


#### Reserve discharge path

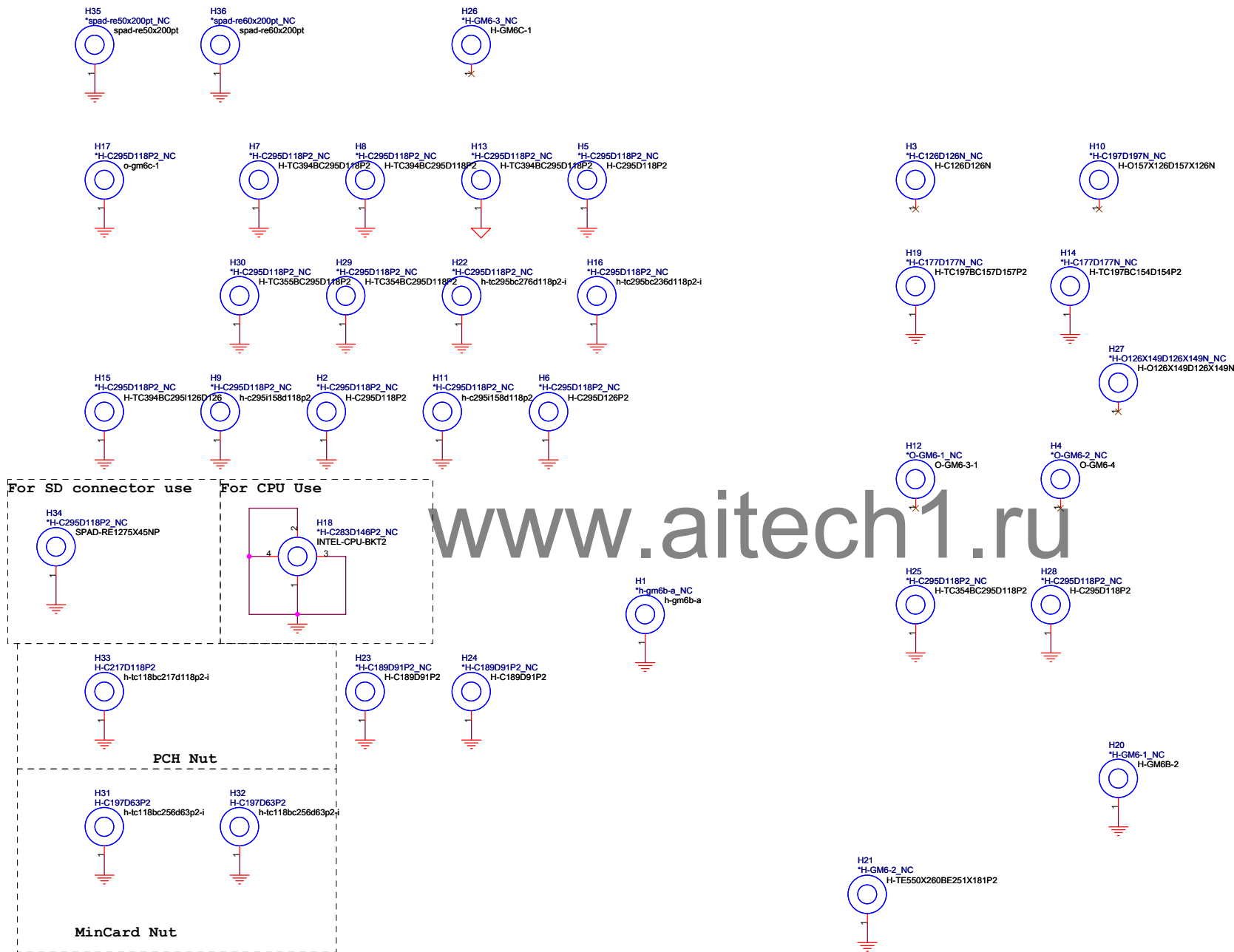


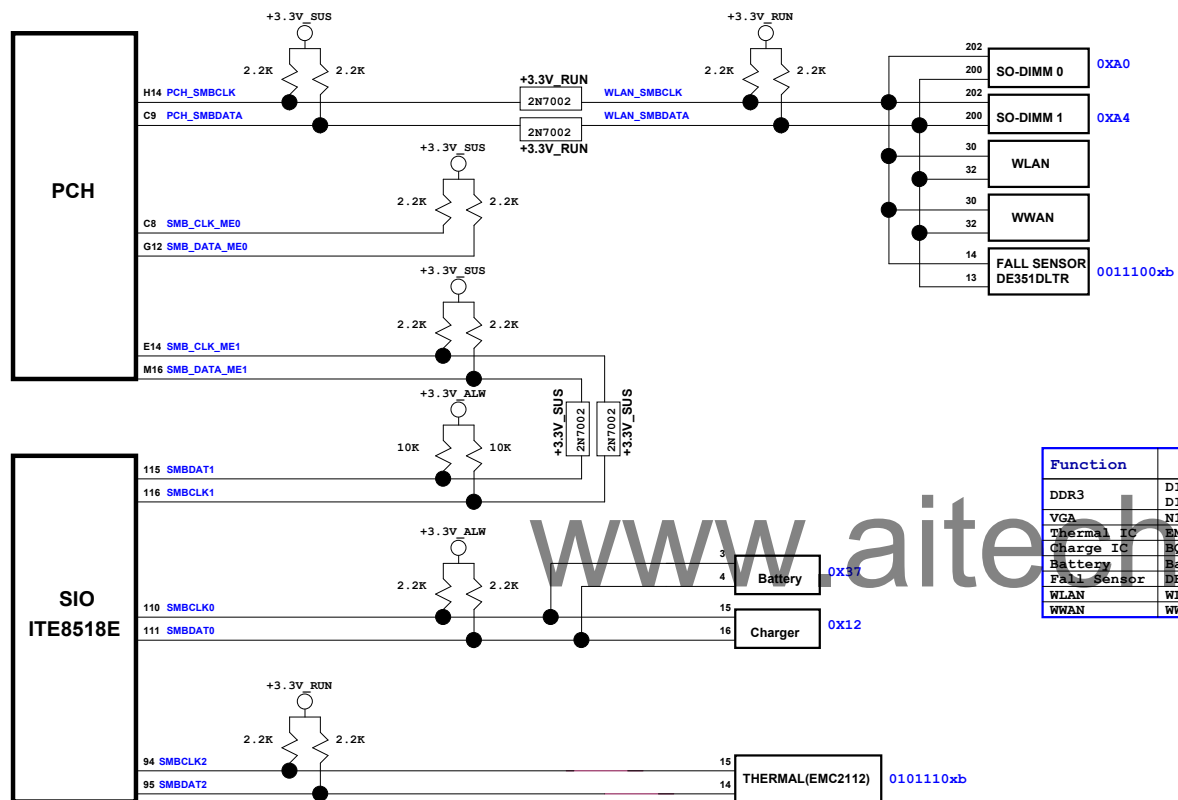


10

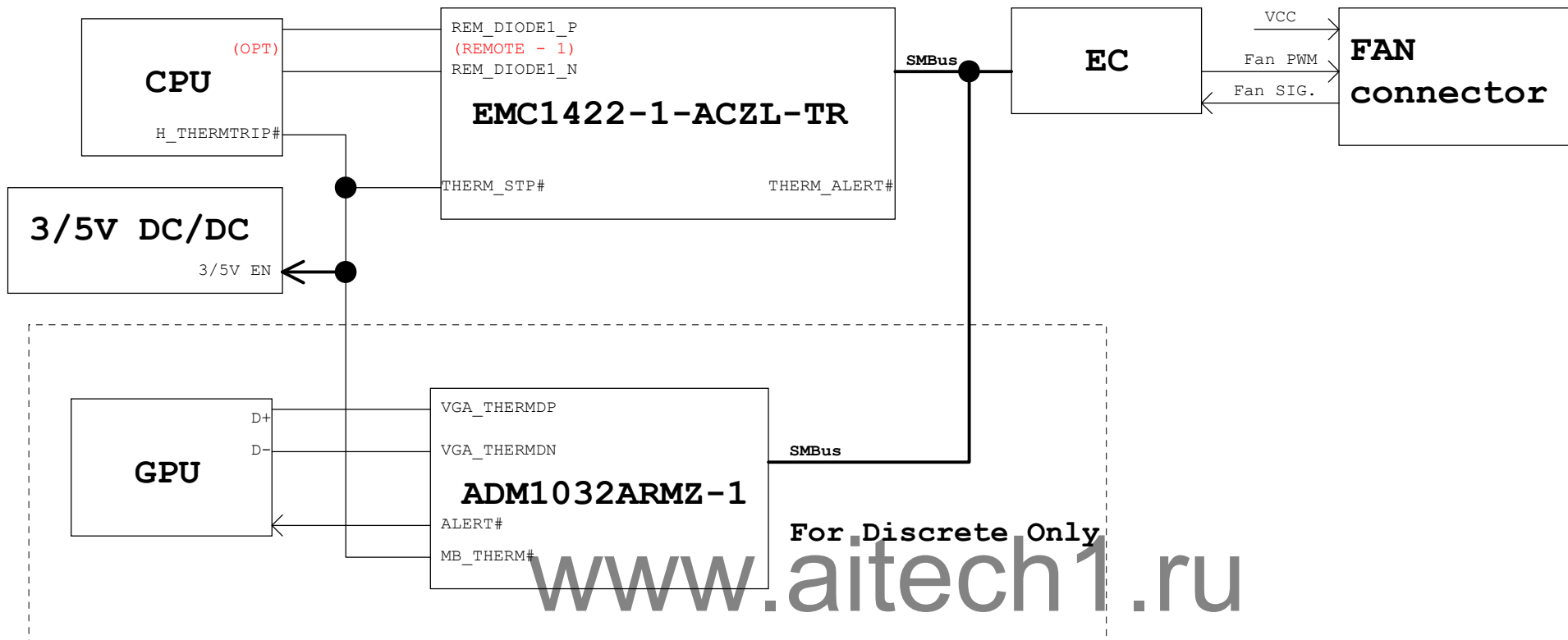


P07

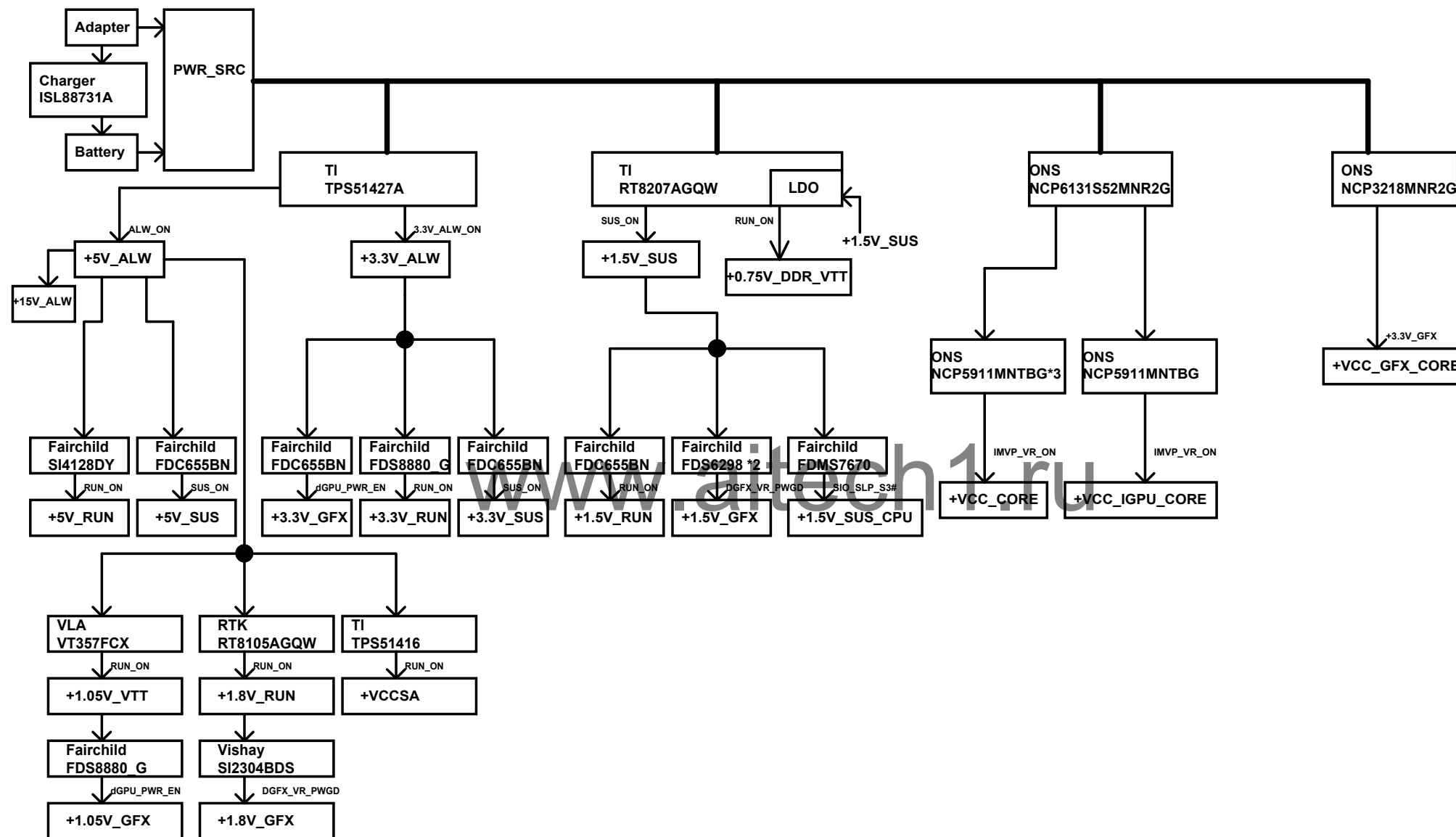




Function	IC	SMBus Address
DDR3	DIMM0	A0
	DIMM1	A4
VGA	N11P	9E
Thermal IC	EMC2112	0101110xb
Charge IC	BQ24765RUVR	0x12
Battery	Battery	0X37
Fall Sensor	DE351DLTR	0101110xb
WLAN	WLAN Module	X
WWAN	WWAN Module	X



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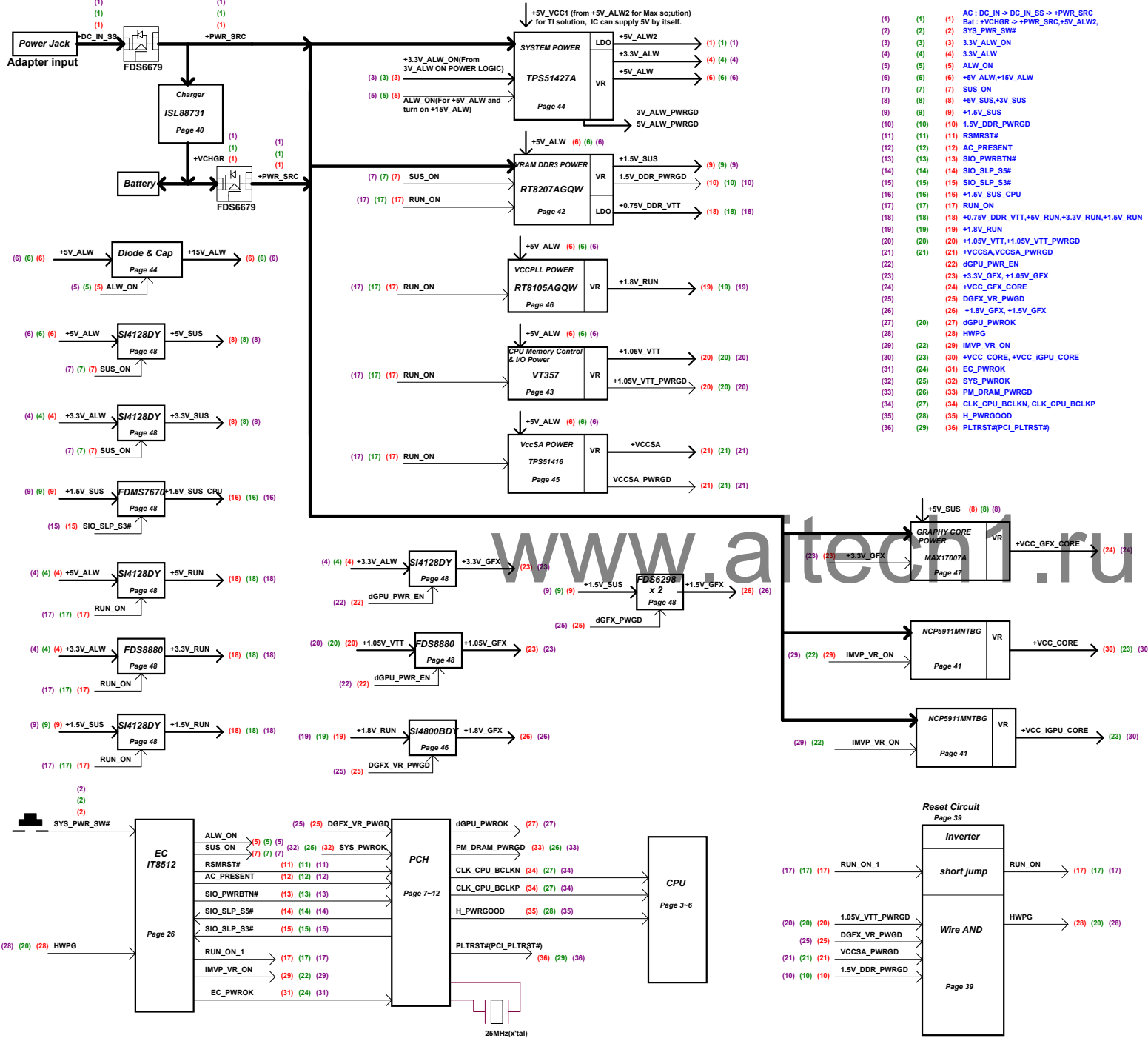


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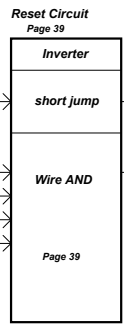
**PROJECT : GM6C MLK DIS**

Size	Document Number	Rev
		1A
<b>Power Block Diagram</b>		
Date: Friday, January 07, 2011	Sheet 55 of 59	

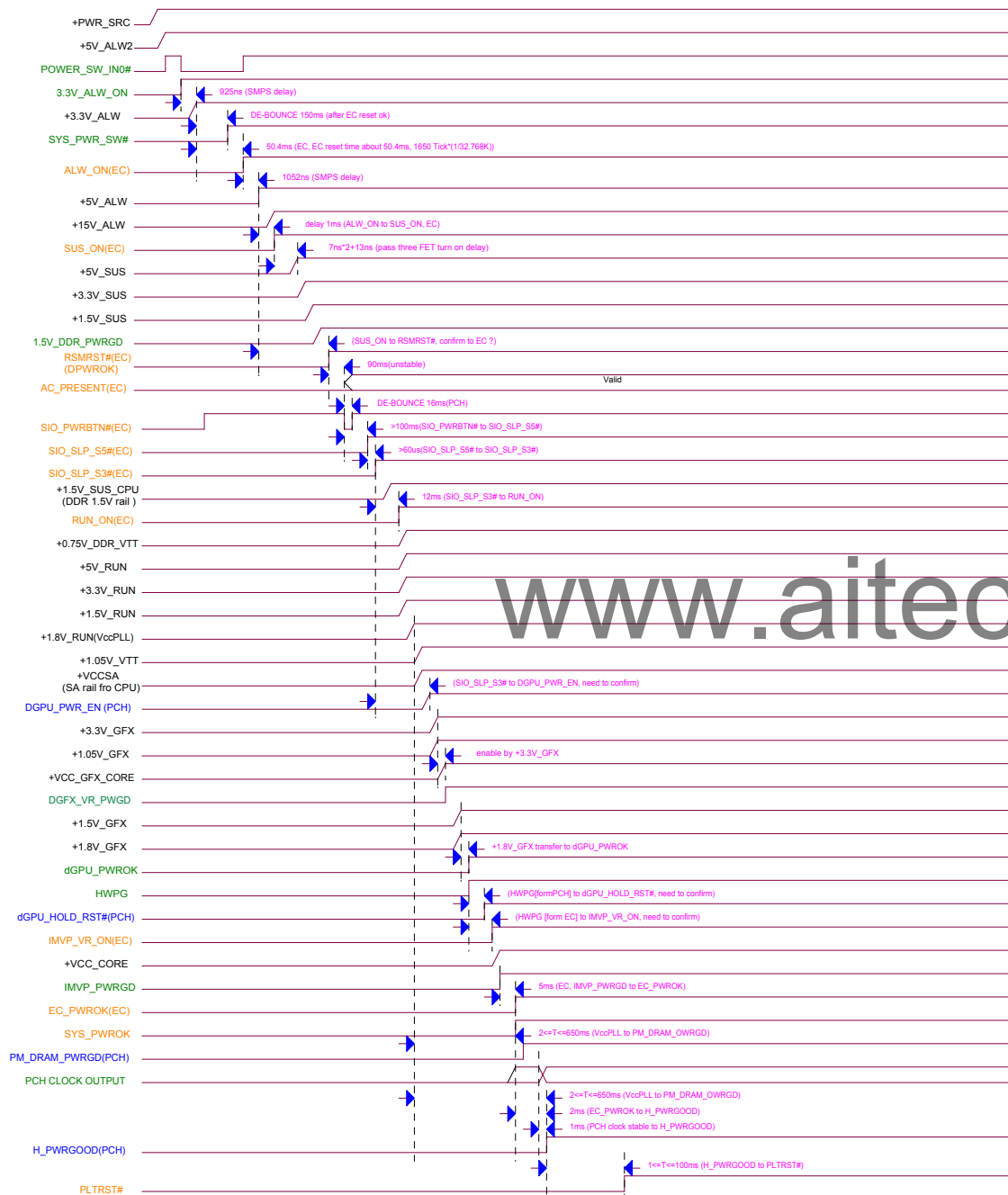
GM6C-MLK Power Design Block Diagram



OPTIMUS	UMA	DIS
(1)	(1)	AC : DC_IN -> DC_IN_SS -> +PWR_SRC
(2)	(2)	Bat : +VCHGR -> +PWR_SRC, +5V_ALW2,
(3)	(3)	SYS_PWR_SW#
(4)	(4)	3.3V_ALW_ON
(5)	(5)	3.3V_ALW
(6)	(6)	ALW_ON
(7)	(7)	+5V_ALW, +15V_ALW
(8)	(8)	SUS_ON
(9)	(9)	+5V_SUS, +3V_SUS
(10)	(10)	+1.5V_SUS
(11)	(11)	1.5V_DDR_PWRGD
(12)	(12)	RSMRST#
(13)	(13)	AC_PRESENT
(14)	(14)	SIO_PWRBTN#
(15)	(15)	SIO_SLP_S#
(16)	(16)	SIO_SLP_S3#
(17)	(17)	+1.5V_SUS_CPU
(18)	(18)	RUN_ON
(19)	(19)	+0.75V_DDR_VTT, +5V_RUN, +3.3V_RUN, +1.5V_RUN
(20)	(20)	+1.8V_RUN
(21)	(21)	+1.05V_VTT, +1.05V_VTT_PWRGD
(22)	(22)	+VCCSA, VCCSA_PWRGD
(23)	(23)	dGPU_PWR_EN
(24)	(24)	+3.3V_GFX, +1.05V_GFX
(25)	(25)	+VCC_GFX_CORE
(26)	(26)	DGFX_VR_PWGD
(27)	(27)	+1.8V_GFX, +1.5V_GFX
(28)	(28)	dGPU_PWRGOK
(29)	(29)	IMVP_VR_ON
(30)	(30)	+VCC_CORE, +VCC_IGPU_CORE
(31)	(31)	EC_PWROK
(32)	(32)	SYS_PWROK
(33)	(33)	PM_DRAM_PWRGD
(34)	(34)	CLK_CPU_BCLKN, CLK_CPU_BCLKP
(35)	(35)	H_PWRGOOD
(36)	(36)	PLTRST#(PCI_PLTRST#)

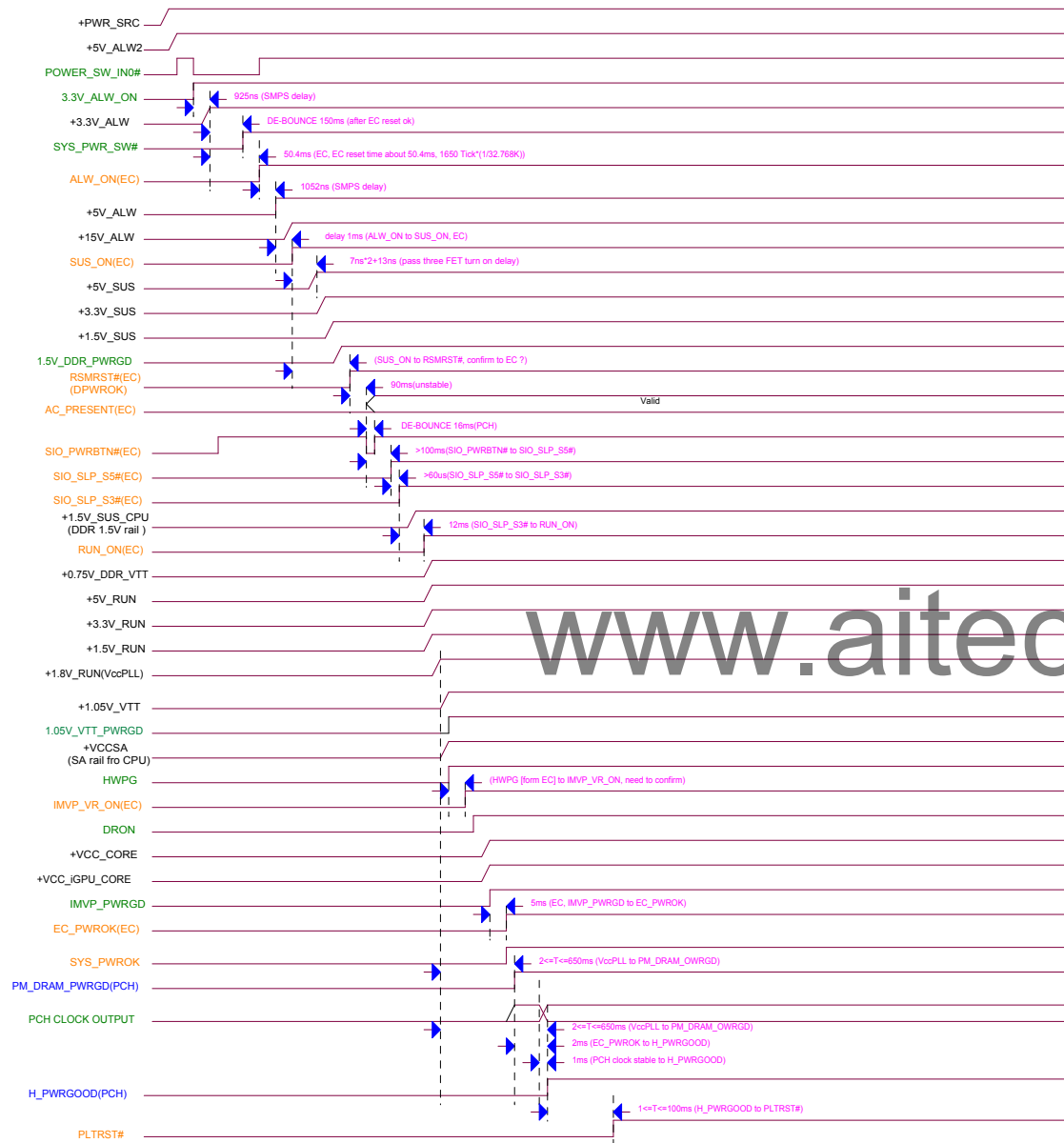


# GM6C\_MLK\_DIS Power on Timing(BATTERY MODE)



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# GM6C\_MLK\_UMA Power on Timing(BATTERY MODE)



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# GM6C\_MLK\_OPTIMUS Power on Timing(BATTERY MODE)

